


GA-990FXA-UD3

Revision : 4.01

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11	RD990 SYSTEM I/F, STRAPS
12	RD990 POWER & GND
13	ICS9LPRS477
14	ATI SB950 PCIE/PCI/CPU/LPC
15	ATI SB950 ACPI/USB/GPIO/AUDIO
16	ATI SB950 SATA/SPI/IDE/HWM
17	ATI SB950 POWER & GND
18	PCI EXPRESS x16 ,x1
19	PCI EXPRESS x16 ,X4
20	PCI SLOT , PCIEx4
21	ITE 8728EX ,Dual_BIOS ,HWM ,KB/MS
22	F_USB
23	ALC889
24	AUDIO JACK
25	FAN/HWMO/COM

[illegible]

			
Title			
COVER SHEET			
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Component value change history

4 Layer, 4mil 50ohm +/- 15% X

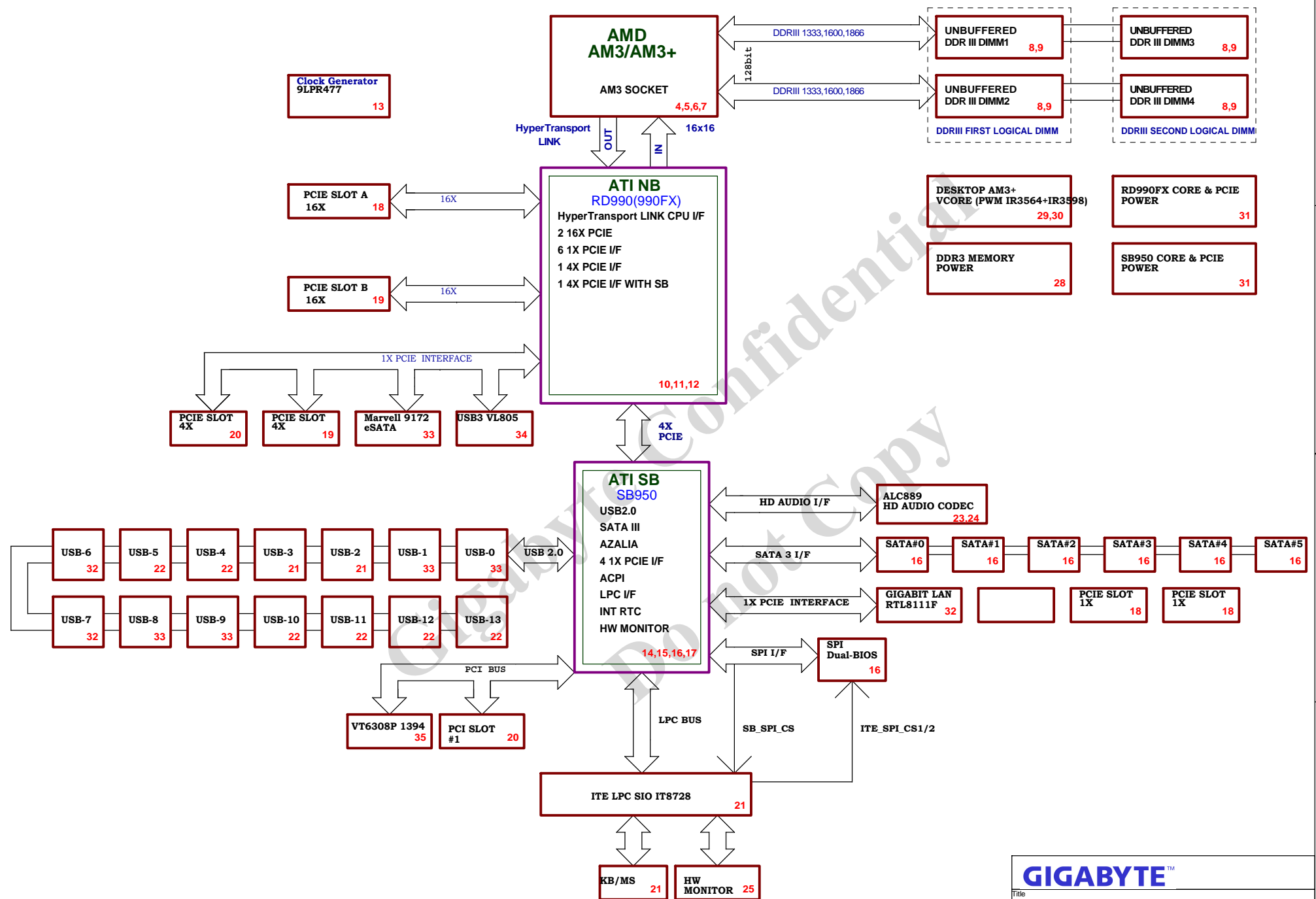
Version: 4.01

P-Code:
U98145-0

[illegible]

Circuit or PCB layout change for next version

[illegible]



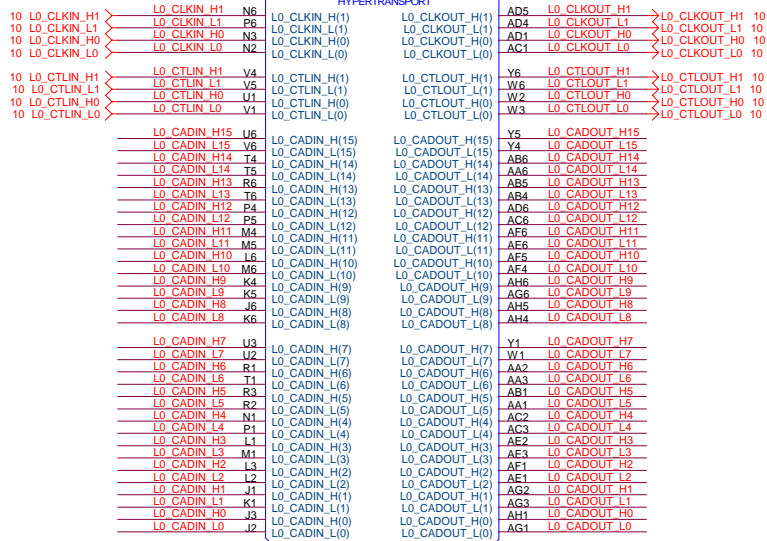
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BLOCK DIAGRAM			
Title	BLOCK DIAGRAM		
Size	Document Number	Rev	
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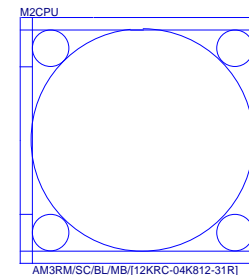
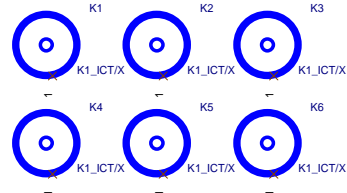
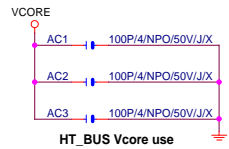
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 L0_CADIN_H[0..15] <L0_CADIN_H[0..15] 10
 L0_CADOUT_L[0..15] <L0_CADOUT_L[0..15] 10
 L0_CADOUT_H[0..15] <L0_CADOUT_H[0..15] 10

M2CPUA

HYPERTRANSPORT

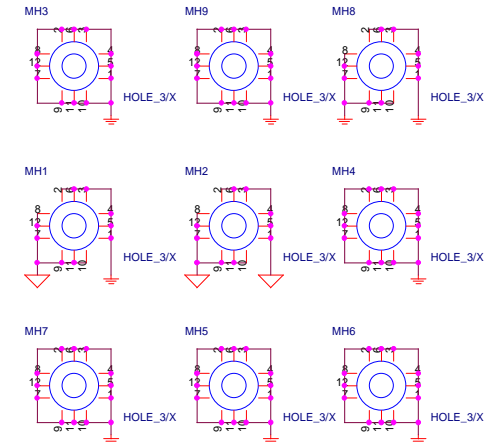


CPU-SK/941AM3/S/GF/[10SC1-A01942-01R_10SC1-A01942-02R]

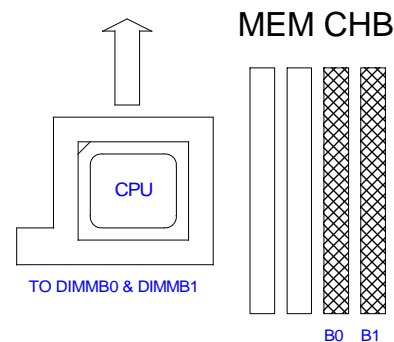
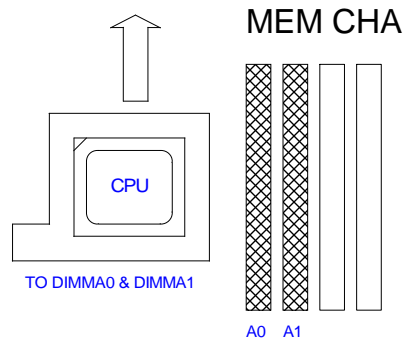
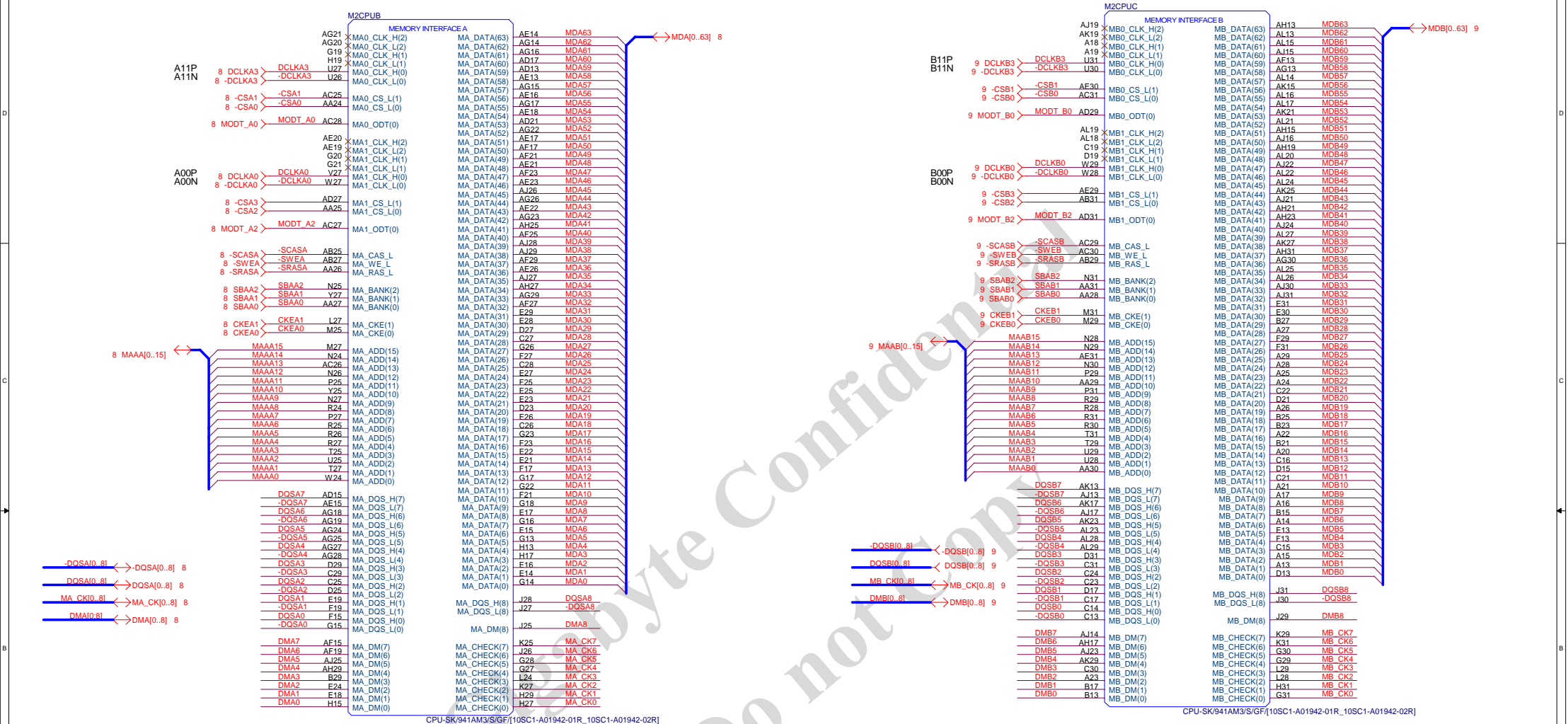


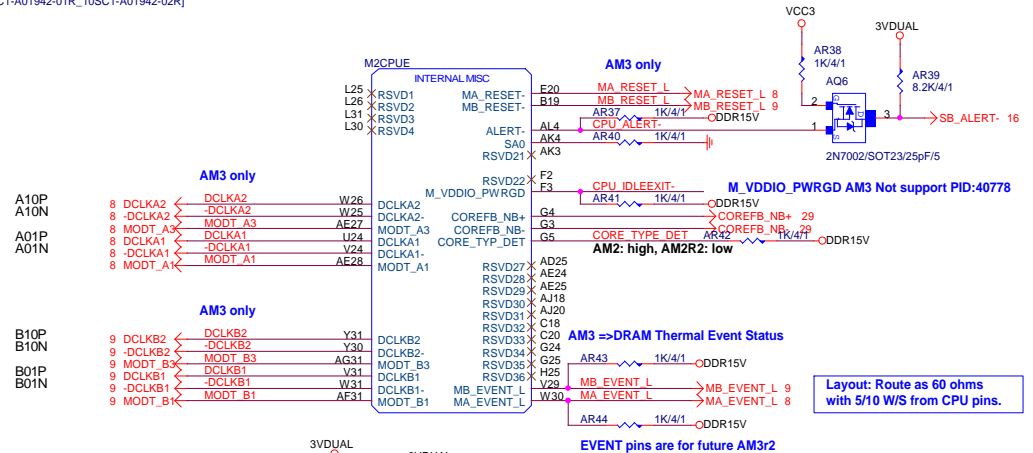
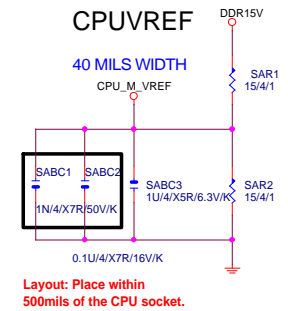
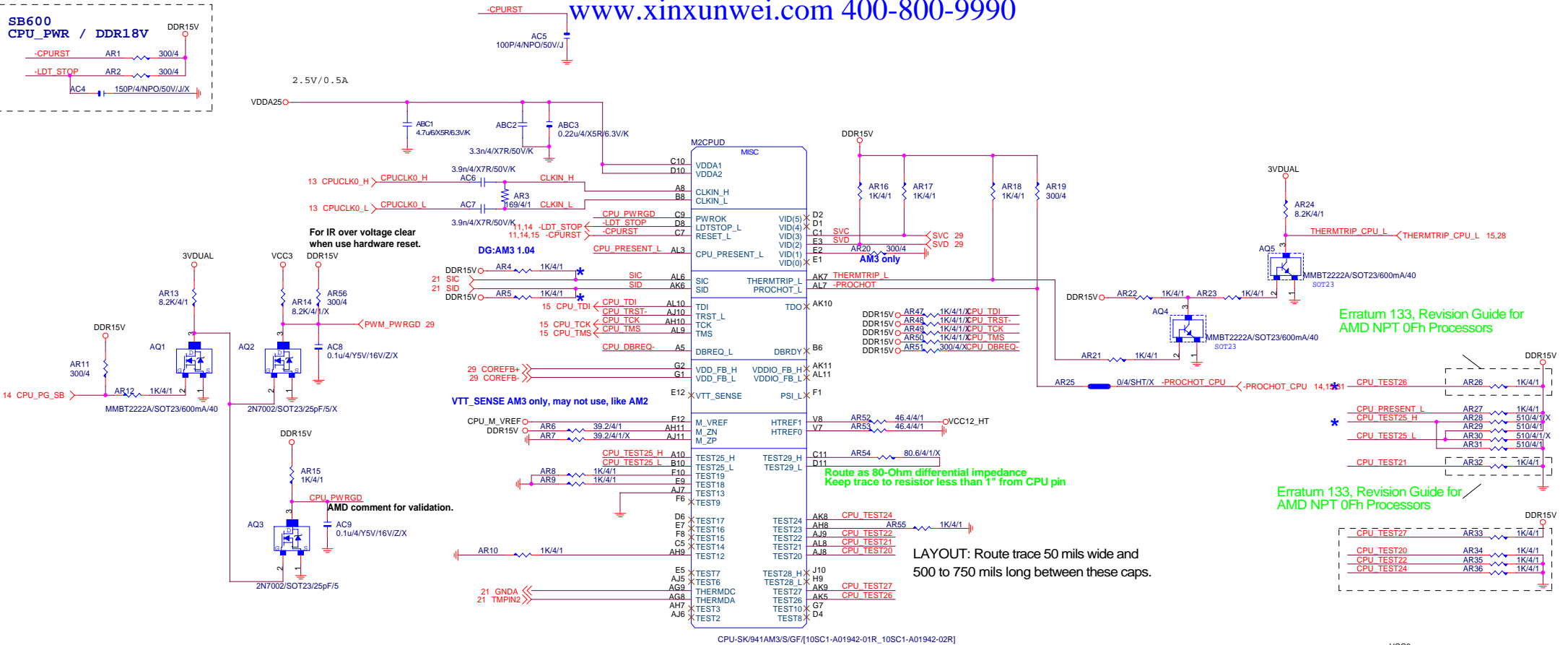
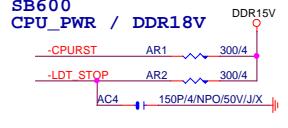
CPU_VDD_RUN = VCORE
 CPU_VDDA_RUN = VDDA25
 VLDT_RUN = VCC12_HT
 CPU_VDDIO_SUS = DDR15V
 CPU_VDDR = CPU_VDDR12

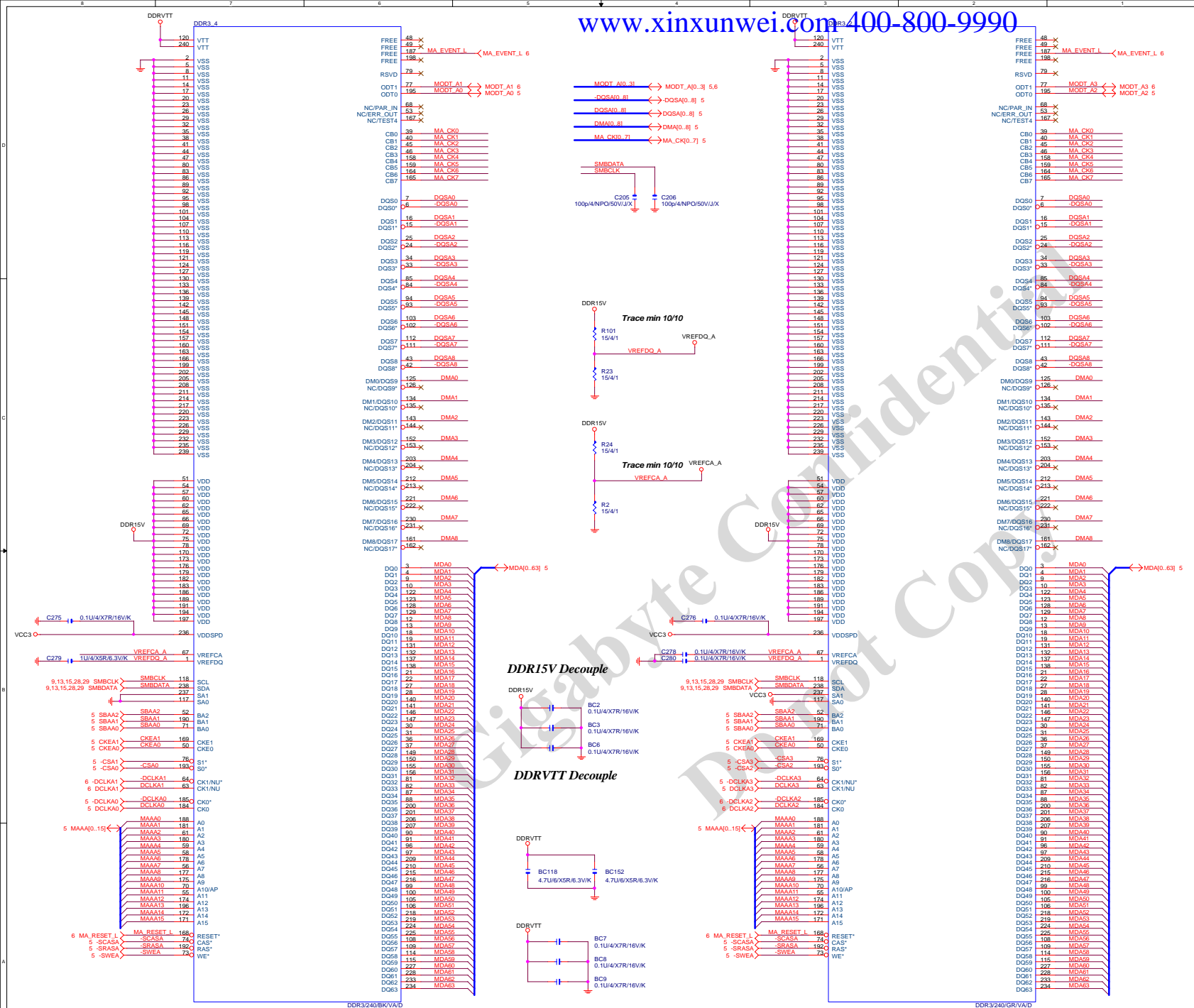
VLDT_A = VCC12_HT
 VLDT_B = HT12B

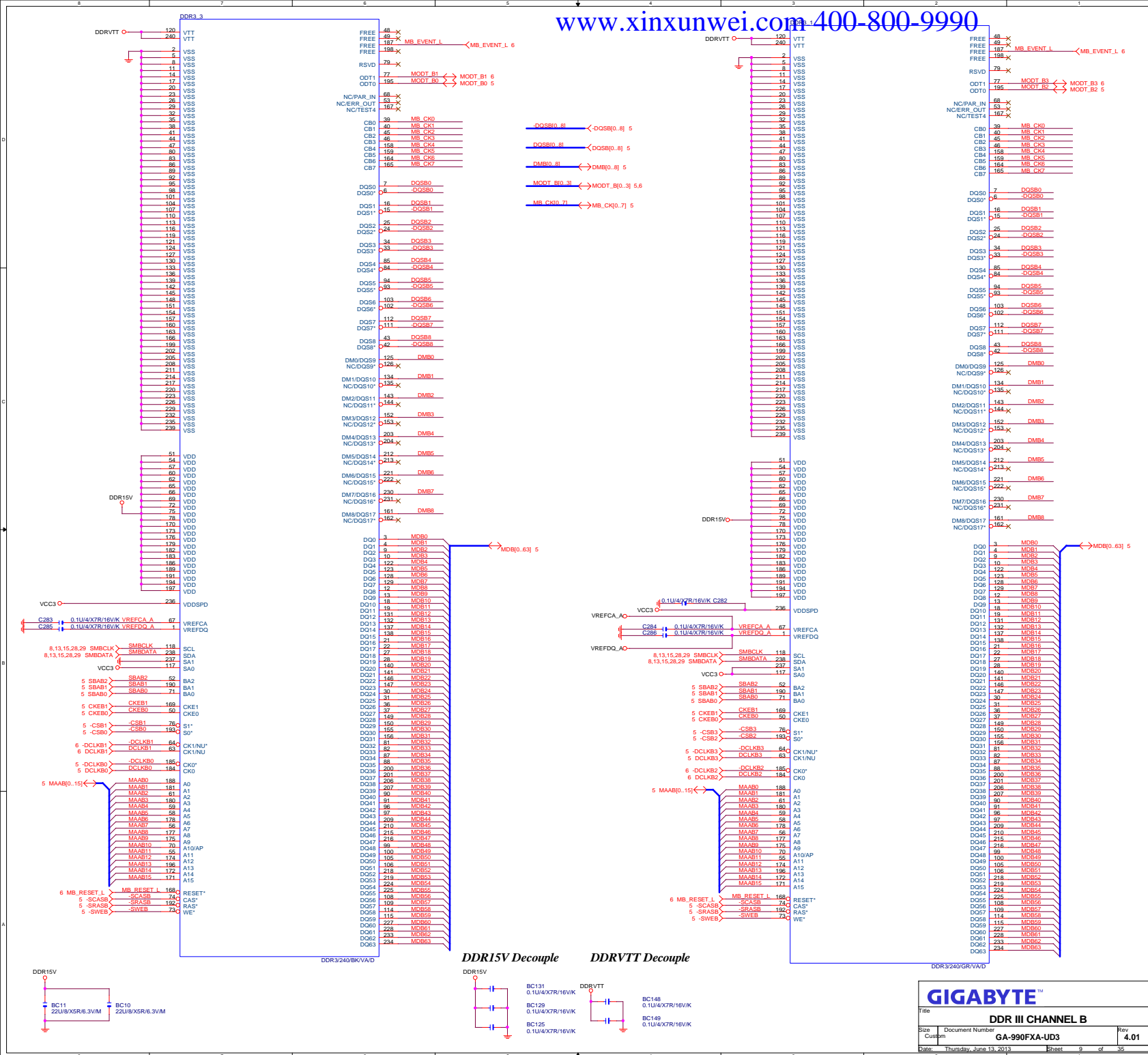


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U3A

PART 1/5

PART 2/5

L0_CADOUT_H15	T25	HT_RXCAD15P	HT_TXCAD15P	N23	L0_CADIN_H15
L0_CADOUT_L15	T24	HT_RXCAD15N	HT_TXCAD15N	N24	L0_CADIN_L15
L0_CADOUT_H14	U24	HT_RXCAD14P	HT_TXCAD14P	M25	L0_CADIN_H14
L0_CADOUT_L14	U23	HT_RXCAD14N	HT_TXCAD14N	M24	L0_CADIN_L14
L0_CADOUT_H13	V25	HT_RXCAD13P	HT_TXCAD13P	L23	L0_CADIN_H13
L0_CADOUT_L13	V24	HT_RXCAD13N	HT_TXCAD13N	L24	L0_CADIN_L13
L0_CADOUT_H12	W24	HT_RXCAD12P	HT_TXCAD12P	K24	L0_CADIN_H12
L0_CADOUT_L12	W23	HT_RXCAD12N	HT_TXCAD12N	K25	L0_CADIN_L12
L0_CADOUT_H11	AA24	HT_RXCAD11P	HT_TXCAD11P	H24	L0_CADIN_H11
L0_CADOUT_L11	AA23	HT_RXCAD11N	HT_TXCAD11N	H25	L0_CADIN_L11
L0_CADOUT_H10	AB25	HT_RXCAD10P	HT_TXCAD10P	G23	L0_CADIN_H10
L0_CADOUT_L10	AB24	HT_RXCAD10N	HT_TXCAD10N	G24	L0_CADIN_L10
L0_CADOUT_H9	AC24	HT_RXCAD9P	HT_TXCAD9P	F24	L0_CADIN_H9
L0_CADOUT_L9	AC23	HT_RXCAD9N	HT_TXCAD9N	F25	L0_CADIN_L9
L0_CADOUT_H8	AD25	HT_RXCAD8P	HT_TXCAD8P	E23	L0_CADIN_H8
L0_CADOUT_L8	AD24	HT_RXCAD8N	HT_TXCAD8N	E24	L0_CADIN_L8
L0_CADOUT_H7	T28	HT_RXCAD7P	HT_TXCAD7P	N26	L0_CADIN_H7
L0_CADOUT_L7	T27	HT_RXCAD7N	HT_TXCAD7N	N27	L0_CADIN_L7
L0_CADOUT_H6	U27	HT_RXCAD6P	HT_TXCAD6P	M27	L0_CADIN_H6
L0_CADOUT_L6	U26	HT_RXCAD6N	HT_TXCAD6N	M28	L0_CADIN_L6
L0_CADOUT_H5	V28	HT_RXCAD5P	HT_TXCAD5P	L26	L0_CADIN_H5
L0_CADOUT_L5	V27	HT_RXCAD5N	HT_TXCAD5N	L27	L0_CADIN_L5
L0_CADOUT_H4	W27	HT_RXCAD4P	HT_TXCAD4P	K27	L0_CADIN_H4
L0_CADOUT_L4	W26	HT_RXCAD4N	HT_TXCAD4N	K28	L0_CADIN_L4
L0_CADOUT_H3	AA27	HT_RXCAD3P	HT_TXCAD3P	J28	L0_CADIN_H3
L0_CADOUT_L3	AA26	HT_RXCAD3N	HT_TXCAD3N	J29	L0_CADIN_L3
L0_CADOUT_H2	AB28	HT_RXCAD2P	HT_TXCAD2P	G26	L0_CADIN_H2
L0_CADOUT_L2	AB27	HT_RXCAD2N	HT_TXCAD2N	G27	L0_CADIN_L2
L0_CADOUT_H1	AC27	HT_RXCAD1P	HT_TXCAD1P	F27	L0_CADIN_H1
L0_CADOUT_L1	AC26	HT_RXCAD1N	HT_TXCAD1N	F28	L0_CADIN_L1
L0_CADOUT_H0	AD28	HT_RXCAD0P	HT_TXCAD0P	E26	L0_CADIN_H0
L0_CADOUT_L0	AD27	HT_RXCAD0N	HT_TXCAD0N	E27	L0_CADIN_L0

4 L0_CLKOUT_H1	L0_CLKOUT_H1	Y25	HT_RXCLK1P	HT_TXCLK1P	J23	L0_CLKIN_H1	L0_CLKIN_H1	4
4 L0_CLKOUT_L1	L0_CLKOUT_L1	Y24	HT_RXCLK1N	HT_TXCLK1N	J24	L0_CLKIN_L1	L0_CLKIN_L1	4
4 L0_CLKOUT_H0	L0_CLKOUT_H0	Y28	HT_RXCLK0P	HT_TXCLK0P	J26	L0_CLKIN_H0	L0_CLKIN_H0	4
4 L0_CLKOUT_L0	L0_CLKOUT_L0	Y27	HT_RXCLK0N	HT_TXCLK0N	J27	L0_CLKIN_L0	L0_CLKIN_L0	4
4 L0_CTOUT_H1	L0_CTOUT_H1	R24	HT_RXCTL1P	HT_TXCTL1P	P24	L0_CTLIN_H1	L0_CTLIN_H1	4
4 L0_CTOUT_L1	L0_CTOUT_L1	R23	HT_RXCTL1N	HT_TXCTL1N	P25	L0_CTLIN_L1	L0_CTLIN_L1	4
4 L0_CTOUT_H0	L0_CTOUT_H0	R27	HT_RXCTL0P	HT_TXCTL0P	P27	L0_CTLIN_H0	L0_CTLIN_H0	4
4 L0_CTOUT_L0	L0_CTOUT_L0	R26	HT_RXCTL0N	HT_TXCTL0N	P28	L0_CTLIN_L0	L0_CTLIN_L0	4

SNR0	1.21K/4/1	HT_RXCALN	D25	HT_RXCALP	D28	HT_TXCALN	NR1	1.21K/4/1
		HT_RXCALN	D24	HT_RXCALN	D27	HT_TXCALN		

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L0_CADIN_L10_15]	L0_CADIN_L10_15]	4

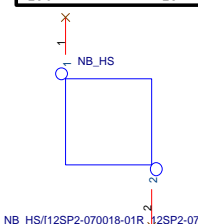
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4 L0_CADOUT_L10_15]	L0_CADOUT_L10_15]	4
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EXP_A_RXP10_15]	EXP_A_RXP10_15]	18
EXP_A_RXN10_15]	EXP_A_RXN10_15]	18
EXP_A_TXP10_15]	EXP_A_TXP10_15]	18
EXP_A_TXN10_15]	EXP_A_TXN10_15]	18

EXP_B_TXP10_15]	EXP_B_TXP10_15]	19
EXP_B_TXN10_15]	EXP_B_TXN10_15]	19
EXP_B_RXP10_15]	EXP_B_RXP10_15]	19
EXP_B_RXN10_15]	EXP_B_RXN10_15]	19

N.B HEATSINK



NB_HS[12SP2-070018-01R, 12SP2-070018-02R]/X

EXP_A_RXP15	N6	GPP1_RX15P	N3	EXP_A_TXP15
EXP_A_RXN15	N5	GPP1_RX15N	N2	EXP_A_TXN15
EXP_A_RXP14	M6	GPP1_RX14P	M2	EXP_A_TXP14
EXP_A_RXN14	M4	GPP1_RX14N	M1	EXP_A_TXN14
EXP_A_RXP13	L6	GPP1_RX13P	L3	EXP_A_TXP13
EXP_A_RXN13	L5	GPP1_RX13N	L2	EXP_A_TXN13
EXP_A_RXP12	K6	GPP1_RX12P	K2	EXP_A_TXP12
EXP_A_RXN12	K4	GPP1_RX12N	K1	EXP_A_TXN12
EXP_A_RXP11	J6	GPP1_RX11P	J3	EXP_A_TXP11
EXP_A_RXN11	J5	GPP1_RX11N	J2	EXP_A_TXN11
EXP_A_RXP10	H6	GPP1_RX10P	H2	EXP_A_TXP10
EXP_A_RXN10	H4	GPP1_RX10N	H1	EXP_A_TXN10
EXP_A_RXP9	G6	GPP1_RX9P	G3	EXP_A_TXP9
EXP_A_RXN9	G5	GPP1_RX9N	G2	EXP_A_TXN9
EXP_A_RXP8	F6	GPP1_RX8P	F2	EXP_A_TXP8
EXP_A_RXN8	F4	GPP1_RX8N	F1	EXP_A_TXN8
EXP_A_RXP7	D2	GPP1_RX7P	E3	EXP_A_TXP7
EXP_A_RXN7	D1	GPP1_RX7N	E2	EXP_A_TXN7
EXP_A_RXP6	B6	GPP1_RX6P	A4	EXP_A_TXP6
EXP_A_RXN6	B5	GPP1_RX6N	B4	EXP_A_TXN6
EXP_A_RXP5	C6	GPP1_RX5P	A6	EXP_A_TXP5
EXP_A_RXN5	E6	GPP1_RX5N	B6	EXP_A_TXN5
EXP_A_RXP4	E7	GPP1_RX4P	B7	EXP_A_TXP4
EXP_A_RXN4	D7	GPP1_RX4N	C7	EXP_A_TXN4
EXP_A_RXP3	E8	GPP1_RX3P	A8	EXP_A_TXP3
EXP_A_RXN3	E8	GPP1_RX3N	B8	EXP_A_TXN3
EXP_A_RXP2	E9	GPP1_RX2P	B9	EXP_A_TXP2
EXP_A_RXN2	E9	GPP1_RX2N	C3	EXP_A_TXN2
EXP_A_RXP1	E10	GPP1_RX1P	A10	EXP_A_TXP1
EXP_A_RXN1	E10	GPP1_RX1N	B10	EXP_A_TXN1
EXP_A_RXP0	E11	GPP1_RX0P	B11	EXP_A_TXP0
EXP_A_RXN0	F11	GPP1_RX0N	C11	EXP_A_TXN0

L0_CLKIN_H1	L0_CLKIN_H1	4
L0_CLKIN_L1	L0_CLKIN_L1	4
L0_CLKIN_H0	L0_CLKIN_H0	4
L0_CLKIN_L0	L0_CLKIN_L0	4

EXP_B_RXP15	AC9	GPP2_RX15P	AF9	EXP_B_TXP15
EXP_B_RXN15	AD9	GPP2_RX15N	AG9	EXP_B_TXN15
EXP_B_RXP14	AE9	GPP2_RX14P	AH9	EXP_B_TXP14
EXP_B_RXN14	AE8	GPP2_RX14N	AH8	EXP_B_TXN14
EXP_B_RXP13	AC7	GPP2_RX13P	AF7	EXP_B_TXP13
EXP_B_RXN13	AD7	GPP2_RX13N	AG7	EXP_B_TXN13
EXP_B_RXP12	AE6	GPP2_RX12P	AH6	EXP_B_TXP12
EXP_B_RXN12	AE5	GPP2_RX12N	AH5	EXP_B_TXN12
EXP_B_RXP11	AE5	GPP2_RX11P	AG4	EXP_B_TXP11
EXP_B_RXN11	AG5	GPP2_RX11N	AH4	EXP_B_TXN11
EXP_B_RXP10	AE2	GPP2_RX10P	AE3	EXP_B_TXP10
EXP_B_RXN10	AE1	GPP2_RX10N	AE2	EXP_B_TXN10
EXP_B_RXP9	AD2	GPP2_RX9P	AC3	EXP_B_TXP9
EXP_B_RXN9	AD1	GPP2_RX9N	AC2	EXP_B_TXN9
EXP_B_RXP8	AB5	GPP2_RX8P	AB2	EXP_B_TXP8
EXP_B_RXN8	AB4	GPP2_RX8N	AB1	EXP_B_TXN8
EXP_B_RXP7	AA6	GPP2_RX7P	AA3	EXP_B_TXP7
EXP_B_RXN7	AA5	GPP2_RX7N	AA2	EXP_B_TXN7
EXP_B_RXP6	Y5	GPP2_RX6P	Y2	EXP_B_TXP6
EXP_B_RXN6	Y4	GPP2_RX6N	Y1	EXP_B_TXN6
EXP_B_RXP5	W6	GPP2_RX5P	W3	EXP_B_TXP5
EXP_B_RXN5	W5	GPP2_RX5N	W2	EXP_B_TXN5
EXP_B_RXP4	V5	GPP2_RX4P	V2	EXP_B_TXP4
EXP_B_RXN4	V4	GPP2_RX4N	V1	EXP_B_TXN4
EXP_B_RXP3	U6	GPP2_RX3P	U3	EXP_B_TXP3
EXP_B_RXN3	U5	GPP2_RX3N	U2	EXP_B_TXN3
EXP_B_RXP2	T5	GPP2_RX2P	T2	EXP_B_TXP2
EXP_B_RXN2	T4	GPP2_RX2N	T1	EXP_B_TXN2
EXP_B_RXP1	RE	GPP2_RX1P	R3	EXP_B_TXP1
EXP_B_RXN1	RE	GPP2_RX1N	R2	EXP_B_TXN1
EXP_B_RXP0	P4	GPP2_RX0P	P2	EXP_B_TXP0
EXP_B_RXN0	P4	GPP2_RX0N	P1	EXP_B_TXN0

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RD990/BGA692

L0_CADIN_H10_15]	L0_CADIN_H10_15]	4
L0_CADIN_L10_15]	L0_CADIN_L10_15]	4

4 L0_CADOUT_H10_15]	L0_CADOUT_H10_15]	4
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4 L0_CADOUT_L10_15]	L0_CADOUT_L10_15]	4
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EXP_A_RXP10_15]	EXP_A_RXP10_15]	18
EXP_A_RXN10_15]	EXP_A_RXN10_15]	18
EXP_A_TXP10_15]	EXP_A_TXP10_15]	18
EXP_A_TXN10_15]	EXP_A_TXN10_15]	18

EXP_B_TXP10_15]	EXP_B_TXP10_15]	19
EXP_B_TXN10_15]	EXP_B_TXN10_15]	19
EXP_B_RXP10_15]	EXP_B_RXP10_15]	19
EXP_B_RXN10_15]	EXP_B_RXN10_15]	19

20 PCIE4_4P	AD11	GPP3_RX9P	AH10	GPP_TX9P	C6	0.1u/4X7R/16V/K	PCIE4_40P	20
20 PCIE4_4N	AD11	GPP3_RX9N	AG10	GPP_TX9N	C5	0.1u/4X7R/16V/K	PCIE4_40N	20
20 PCIE4_3P	AE12	GPP3_RX8P	AE11	GPP_TX8P	C7	0.1u/4X7R/16V/K	PCIE4_30P	20
20 PCIE4_3N	AD12	GPP3_RX8N	AE12	GPP_TX7P	C8	0.1u/4X7R/16V/K	PCIE4_30N	20
20 PCIE4_2P	AD13	GPP3_RX7P	AG12	GPP_TX7N	C11	0.1u/4X7R/16V/K	PCIE4_20P	20
20 PCIE4_2N	AC13	GPP3_RX7N	AG13	GPP_TX6P	C14	0.1u/4X7R/16V/K	PCIE4_10P	20
20 PCIE4_1P	AE14	GPP3_RX6P	AE13	GPP_TX6N	C15	0.1u/4X7R/16V/K	PCIE4_10N	20
20 PCIE4_1N	AD14	GPP3_RX6N	AH14	GPP_TX5P	NC4	0.1u/4X7R/16V/K	PCIE4_10N	20
33 RB_SL_IN	AD15	GPP3_RX5P	AG14	GPP_TX5N	NC3	0.1u/4X7R/16V/K	PCIE4_10N	20
34 UB_USB3_IN	AE16	GPP3_RX4P	AG15	GPP_TX4P	NC6	0.1u/4X7R/16V/K	PCIE4_10N	20
34 UB_USB3_IN	AD16	GPP3_RX4N	AH15	GPP_TX4N	NC5	0.1u/4X7R/16V/K	PCIE4_10N	20
19 PCIE4_4P_SB	AD17	GPP3_RX3P	AG16	GPP_TX3P	NC8	0.1u/4X7R/16V/K	PCIE4_40P_SB	19
19 PCIE4_4N_SB	AD18	GPP3_RX3N	AG17	GPP_TX2P	NC10	0.1u/4X7R/16V/K	PCIE4_30P_SB	19
19 PCIE4_3P_SB	AE18	GPP3_RX2P	AE17	GPP_TX2N	NC9	0.1u/4X7R/16V/K	PCIE4_30N_SB	19
19 PCIE4_2P_SB	AD18	GPP3_RX2N	AH18	GPP_TX1P	NC20	0.1u/4X7R/16V/K	PCIE4_20P_SB	19
19 PCIE4_2N_SB	AD19	GPP3_RX1P	AG18	GPP_TX1N	NC19	0.1u/4X7R/16V/K	PCIE4_20N_SB	19
19 PCIE4_1P_SB	AE19	GPP3_RX0P	AG19	GPP_TX0P	NC2	0.1u/4X7R/16V/K	PCIE4_10P_SB	19
19 PCIE4_1N_SB	AG20	GPP3_RX0N	AE19	GPP_TX0N	NC1	0.1u/4X7R/16V/K	PCIE4_10N_SB	19

14 A_RX3P	AC21	SB_RX3P	SB_TX3P	AG22	A_TX3P	C	NC11	0.1u/4X7R/16V/K	A_TX3P	14
14 A_RX3N	AD21	SB_RX3N	SB_TX3N	AG23	A_TX3N	C	NC12	0.1u/4X7R/16V/K	A_TX3N	14
14 A_RX2P	AE22	SB_RX2P	SB_TX2P	AG24	A_TX2P	C	NC13	0.1u/4X7R/16V/K	A_TX2P	14
14 A_RX2N	AE22	SB_RX2N	SB_TX2N	AG25	A_TX2N	C	NC14	0.1u/4X7R/16V/K	A_TX2N	14
14 A_RX1P	AE25	SB_RX1P	SB_TX1P	AG26	A_TX1P	C	NC15	0.1u/4X7R/16V/K	A_TX1P	14
14 A_RX1N	AG25	SB_RX1N	SB_TX1N	AG27	A_TX1N	C	NC16	0.1u/4X7R/16V/K	A_TX1N	14
14 A_RX0P	AG28	SB_RX0P	SB_TX0P	AG28	A_TX0P	C	NC18	0.1u/4X7R/16V/K	A_TX0P	14
14 A_RX0N	AH28	SB_RX0N	SB_TX0N	AG29	A_TX0N	C	NC17	0.1u/4X7R/16V/K	A_TX0N	14

PCIE_BCALRP	PCIE_BCALRN	PCIE_RCALRP	PCIE_RCALRN	PCIE_TCALRP	PCIE_TCALRN
PCIE_BCALRP	PCIE_BCALRN	PCIE_RCALRP	PCIE_RCALRN	PCIE_TCALRP	PCIE_TCALRN

RD990/BGA692

RD990/BGA692

RD990/BGA692

RD990/BGA692

RD990/BGA692

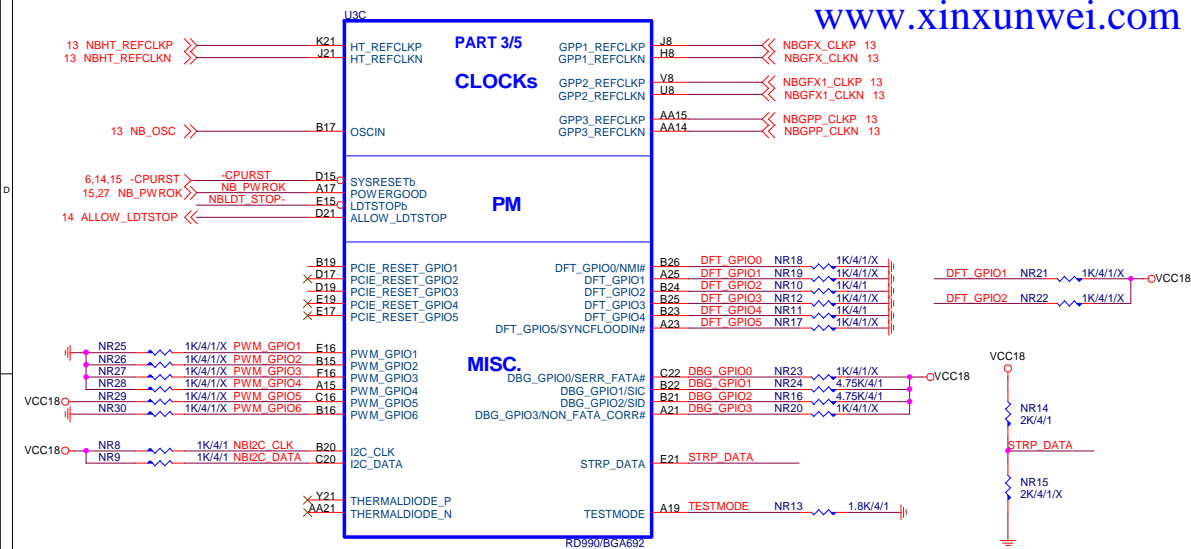
RD990/BGA692

RD990/BGA692

RD990/BGA692

RD990/BGA692

GPP1_RX15P	N3	EXP_A_TXP15
GPP1_RX15N	N2	EXP_A_TXN15
GPP1_RX14P	M2	EXP_A_TXP14
GPP1_RX14N	M1	EXP_A_TXN14
GPP1_RX13P	L3	EXP_A_TXP13
GPP1_RX13N	L2	EXP_A_TXN13
GPP1_RX12P	K2	EXP_A_TXP12
GPP1_RX12N	K1	EXP_A_TXN12
GPP1_RX11P	J3	EXP_A_TXP11
GPP1_RX11N	J2	EXP_A_TXN11
GPP1_RX10P	H2	EXP_A_TXP10
GPP1_RX10N	H1	EXP_A_TXN10
GPP1_RX9P	G3	EXP_A_TXP9
GPP1_RX9N	G2	EXP_A_TXN9
GPP1_RX8P	F2	EXP_A_TXP8
GPP1_RX8N	F1	EXP_A_TXN8
GPP1_RX7P	E3	EXP_A_TXP7
GPP1_RX7N	E2	EXP_A_TXN7
GPP1_RX6P	A4	EXP_A_TXP6
GPP1_RX6N	B4	EXP_A_TXN6
GPP1_RX5P	A6	EXP_A_TXP5
GPP1_RX5N	B6	EXP_A_TXN5
GPP1_RX4P	B7	EXP_A_TXP4
GPP1_RX4N	C7	EXP_A_TXN4
GPP1_RX3P	A8	EXP_A_TXP3
GPP1_RX3N	B8	EXP_A_TXN3
GPP1_RX2P	B9	EXP_A_TXP2
GPP1_RX2N	C3	EXP_A_TXN2
GPP1_RX1P	A10	EXP_A_TXP1
GPP1_RX1N	B10	EXP_A_TXN1</

**DFT_GPIO5: STRAP_DEBUG_BUS_GPIO_ENABLEb**

Enables the Test Debug Bus using GPIO.
1 : Disable (Can still be enabled using nbcfg register access)
0 : Enable

DFT_GPIO[4:2]: STRAP_PCIE_GPP_CFG[2:0]

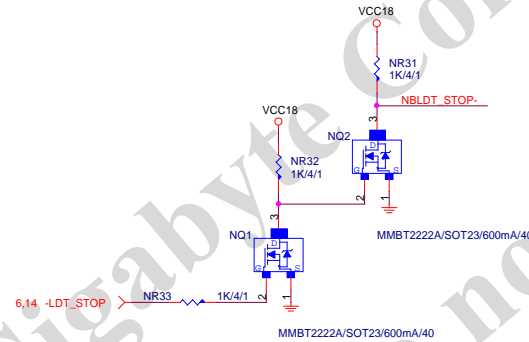
These pin straps are used to configure PCI-E GPP mode.
GPIO4:3:2
000 : 4:2:4 B
001 : 4:1:1:4 C
010 : 1:1:1:1:1:4 L (Hardware Default)
011 : 2:1:1:1:1:4 E
100 : 2:2:1:1:4 K
101 : 2:2:2:4 C2
110 : Hardware default (mode L) or EEPROM
111 : Hardware default (mode L) or EEPROM
101 : 01100
111 : 01011

DFT_GPIO1: LOAD_EEPROM_STRAPS

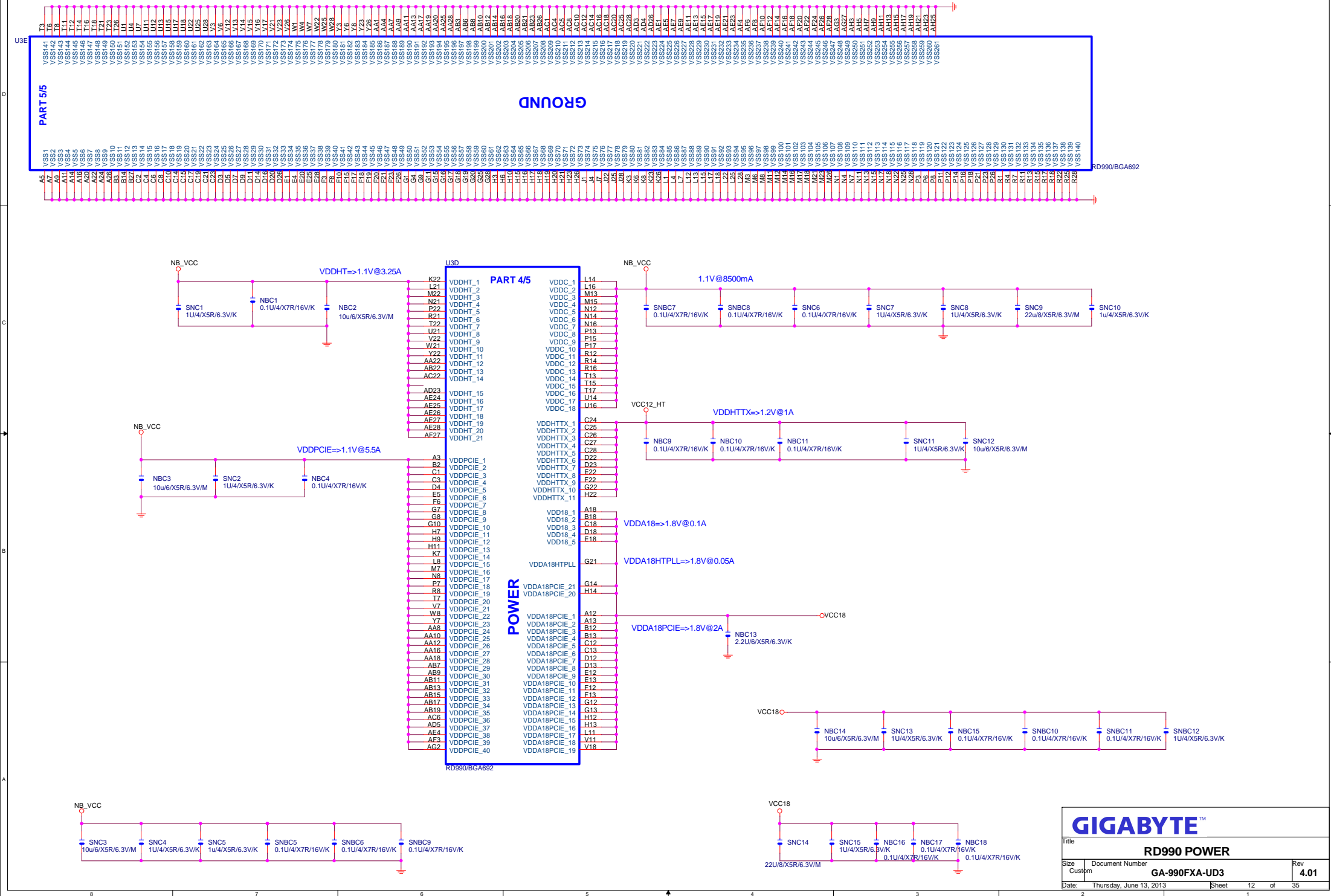
Selects Loading of STRAPS from EPROM
1 : Bypass the loading of EEPROM straps and use Hardware Default Values
0 : I2C Master can load strap values from EEPROM if connected, or use default values if not connected

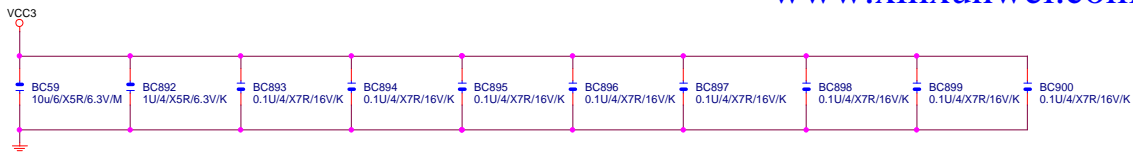
DFT_GPIO0: STRAP_DEBUG_BUS_PCIE_ENABLEb

Enables the Test Debug Bus using PCIE bus
1 : Disable (Can still be enabled using nbcfg register access)
0 : Enable

**GIGABYTE™**

Title		RD990 CLOCK & SYSB I/F	
Size	Document Number	GA-990FXA-UD3	Rev
Custom			4.01
Date:	Thursday, June 13, 2013	Sheet	11 of 35

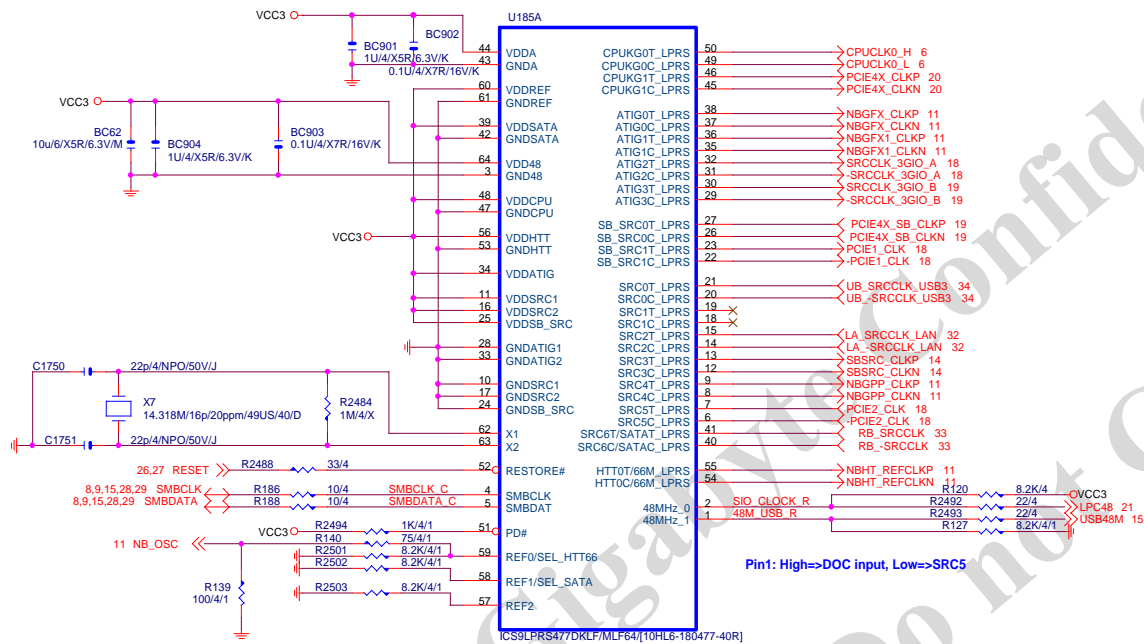




NB CLOCK INPUT TABLE

NB_CLOCKS	RS740	RX780	RS780	
HT_REFCLKP	66M SE(SE)	100M DIFF	100M DIFF	
HT_REFCLKN	NC	100M DIFF	100M DIFF	
REFCLK_P	14M SE (3.3V)	14M SE (1.8V)	14M SE (1.1V)	100M DIFF
REFCLK_N	NC	NC	vref	100M DIFF
GFX_REFCLK*	100M DIFF	100M DIFF	100M DIFF	
GPP_REFCLK	NC	100M DIFF	100M DIFF(OUT)	
GPSSB_REFCLK	100M DIFF	100M DIFF	100M DIFF	

* the GFX_REFCLK input is required for all cases



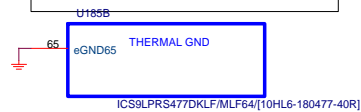
Pin1: High=>DOC input, Low=>SRC5

	OSC_14M_NB
RS740	3.3V 33R serial
RX780	1.8V 82.5R/130R
RS780 (Single-ended)	1.1V 158R/90.9R

REF0/SEL_HTT66	HTT CLOCK
0	100.00 DIFFERENTIAL
1	66.66 SINGLE END

REF1/SEL_SATA	SRC6/SATA
0	100.00 DIFFERENTIAL SPREADING SRC CLOCK
1	100.00 NON-SPREADING DIFFERENTIAL SATA CLOCK

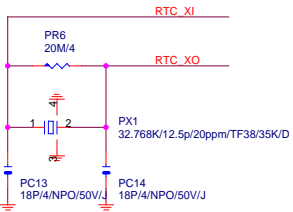
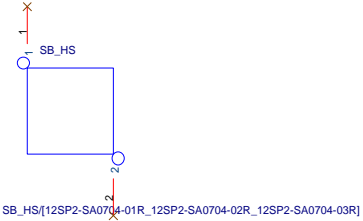
Clock chip has internal serial terminations for differential pairs, external resistors are reserved for debug purpose.



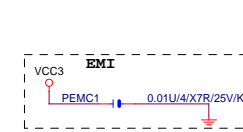
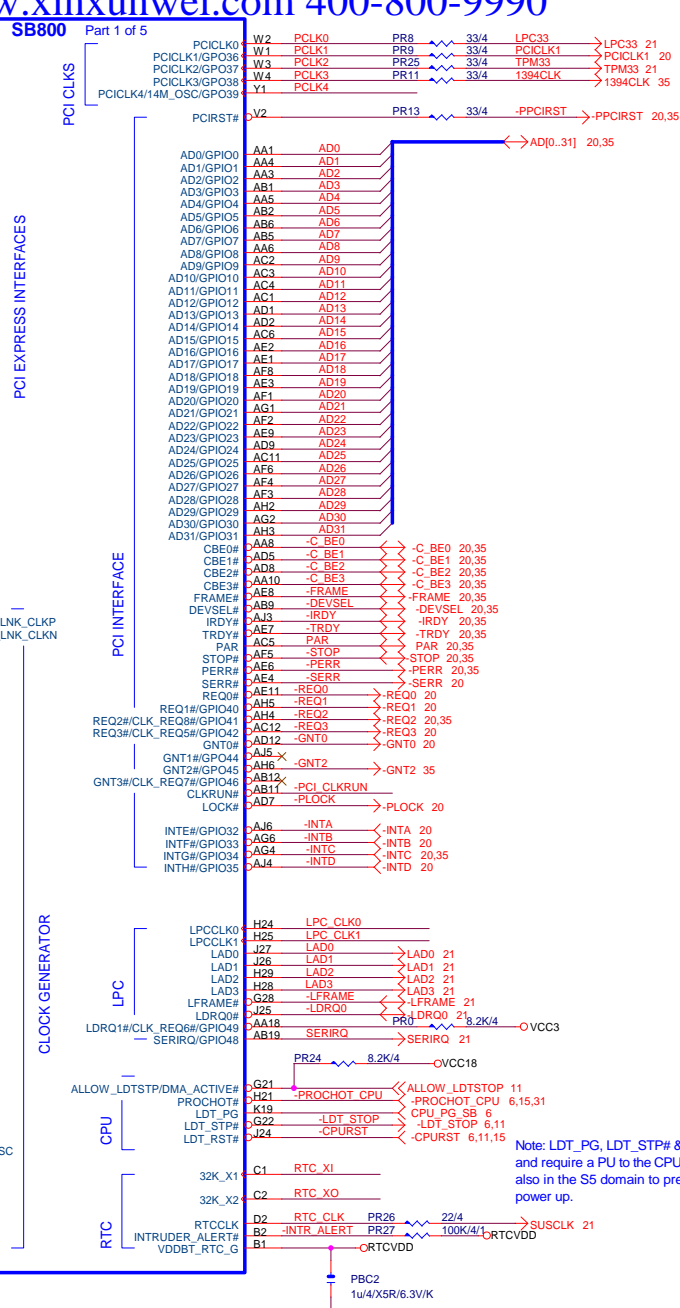
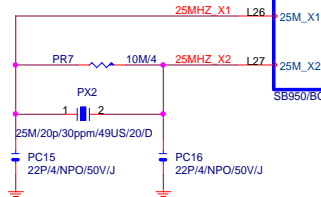
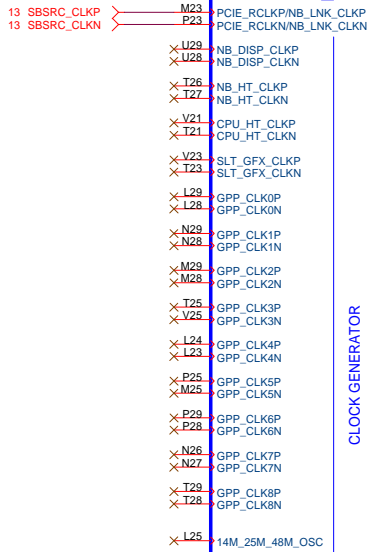
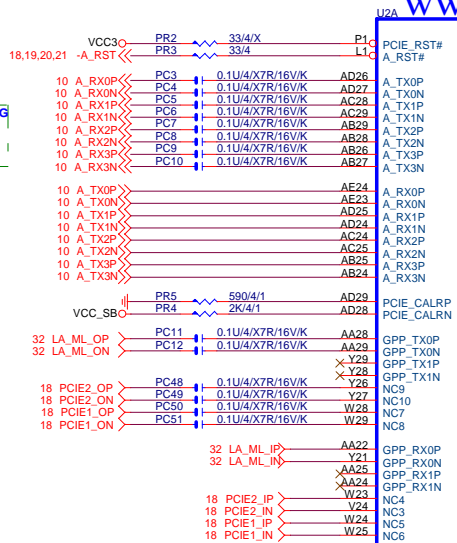
Title			
ICS9LPRS477			
Size	Document Number	Rev	
Custom	GA-990FXA-UD3	4.01	
Date:	Thursday, June 13, 2013	Sheet	13 of 35

PLACE THESE PCIE AC COUPLING
CAPS CLOSE TO SB850

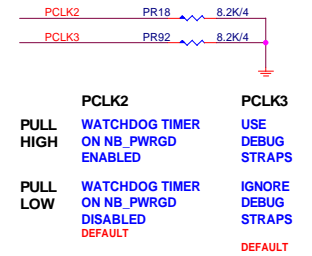
S.B HEATSINK



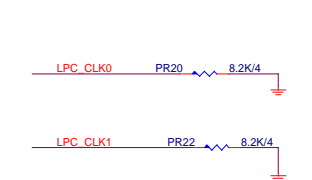
SHW/D0.64*5.08*6.74



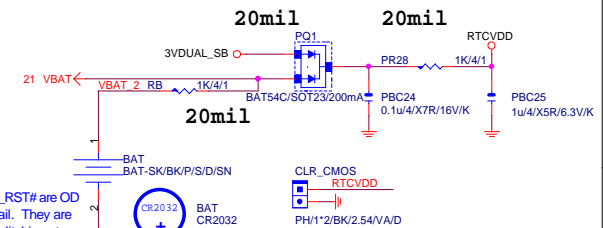
Low: Force PCIE GEN1, Up: Allow PCIE GEN2



BIOS after boot setting
EC AOD-ACC



	LPC_CLK0 Rev.A12	LPC_CLK1
PULL HIGH	IMC ENABLED	CLKGEN ENABLED
PULL LOW	AOD Extreme IMC DISABLED DEFAULT	CLKGEN DISABLED DEFAULT



CLR_CMOS	
SHORT	CLEAR CMOS
OPEN	NORMAL

NOT ADD ICT FOR RTCVDD PIN

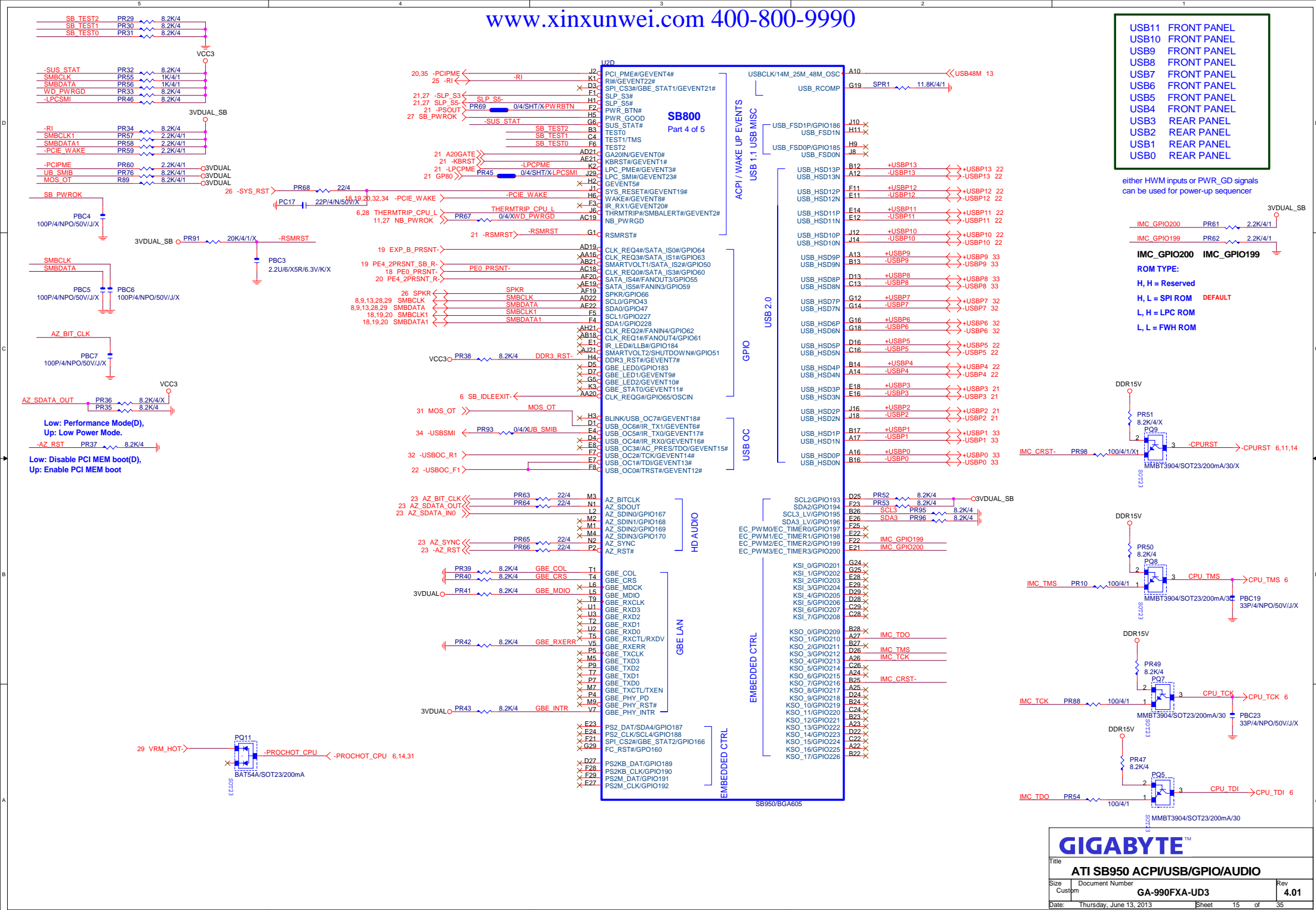
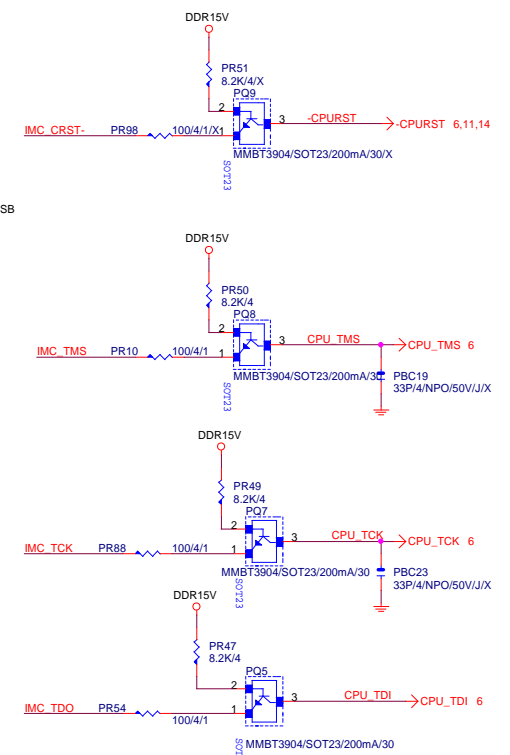
GIGABYTE™

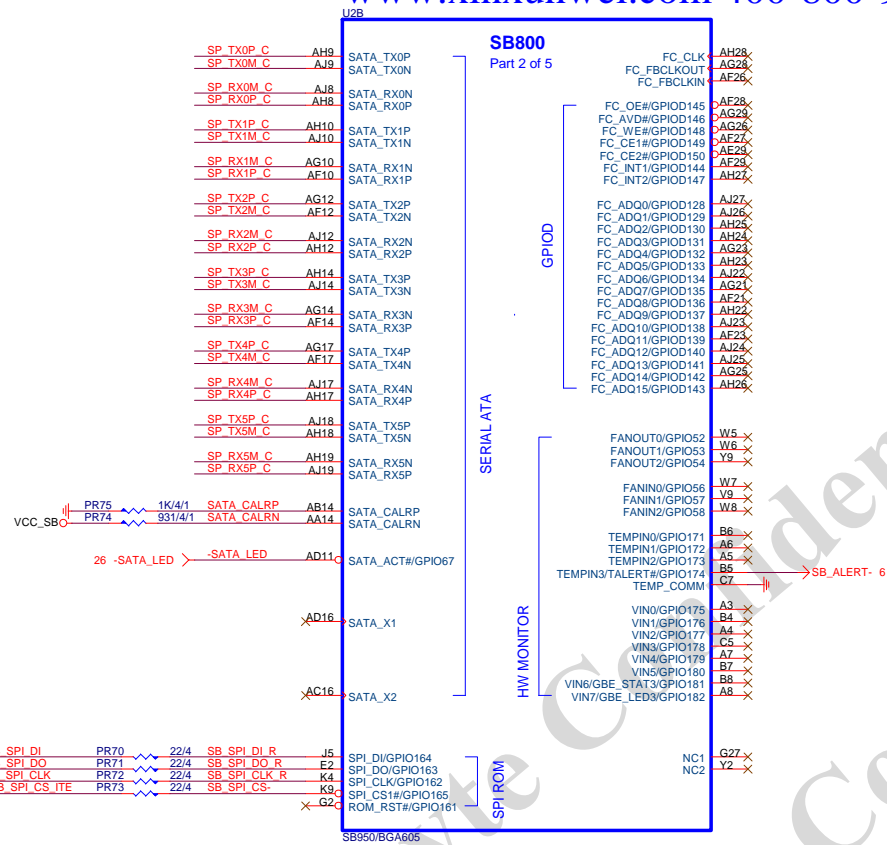
Title			
ATI SB950 PCIE/PCI/CPU/LPC			
Size	Document Number	Rev	
Custom	GA-990FXA-UD3	4.01	
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USB11 FRONT PANEL
 USB10 FRONT PANEL
 USB9 FRONT PANEL
 USB8 FRONT PANEL
 USB7 FRONT PANEL
 USB6 FRONT PANEL
 USB5 FRONT PANEL
 USB4 FRONT PANEL
 USB3 REAR PANEL
 USB2 REAR PANEL
 USB1 REAR PANEL
 USB0 REAR PANEL

either HWM inputs or PWR_GD signals
 can be used for power-up sequencer

IMC_GPIO200 PR61 2.2K/4/1
 IMC_GPIO199 PR62 2.2K/4/1
IMC_GPIO200 IMC_GPIO199
ROM TYPE:
 H, H = Reserved
 L, L = SPI ROM **DEFAULT**
 L, H = LPC ROM
 L, L = FWH ROM





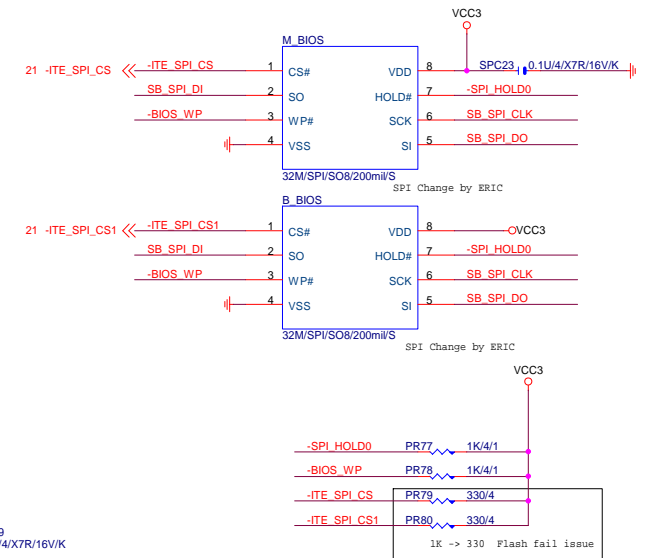
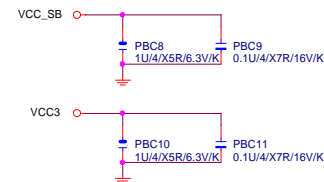
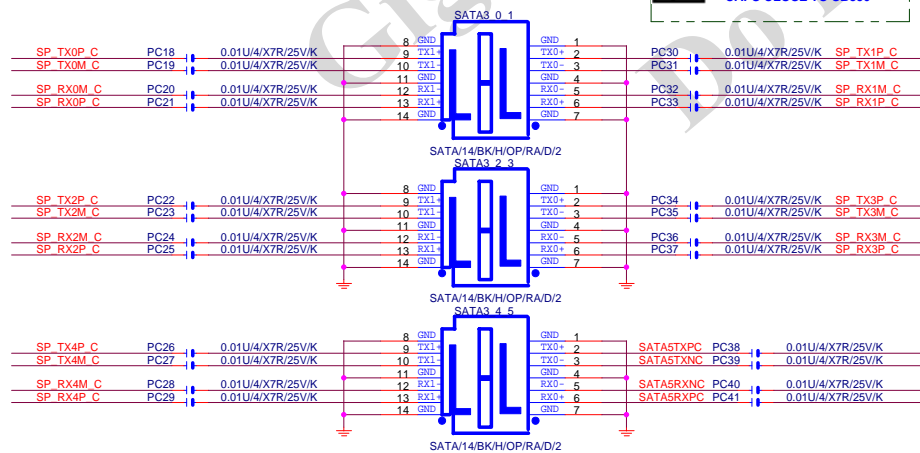
PLACE SATA CAL
RES VERY CLOSE
TO BALL OF U600

NOTE:

R650 IS 1K 1% FOR 25MHz
XTAL, 4.99K 1% FOR 100MHz
INTERNAL CLOCK

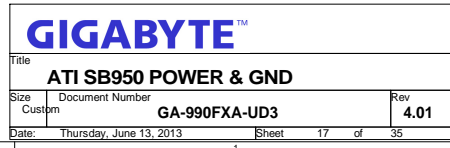


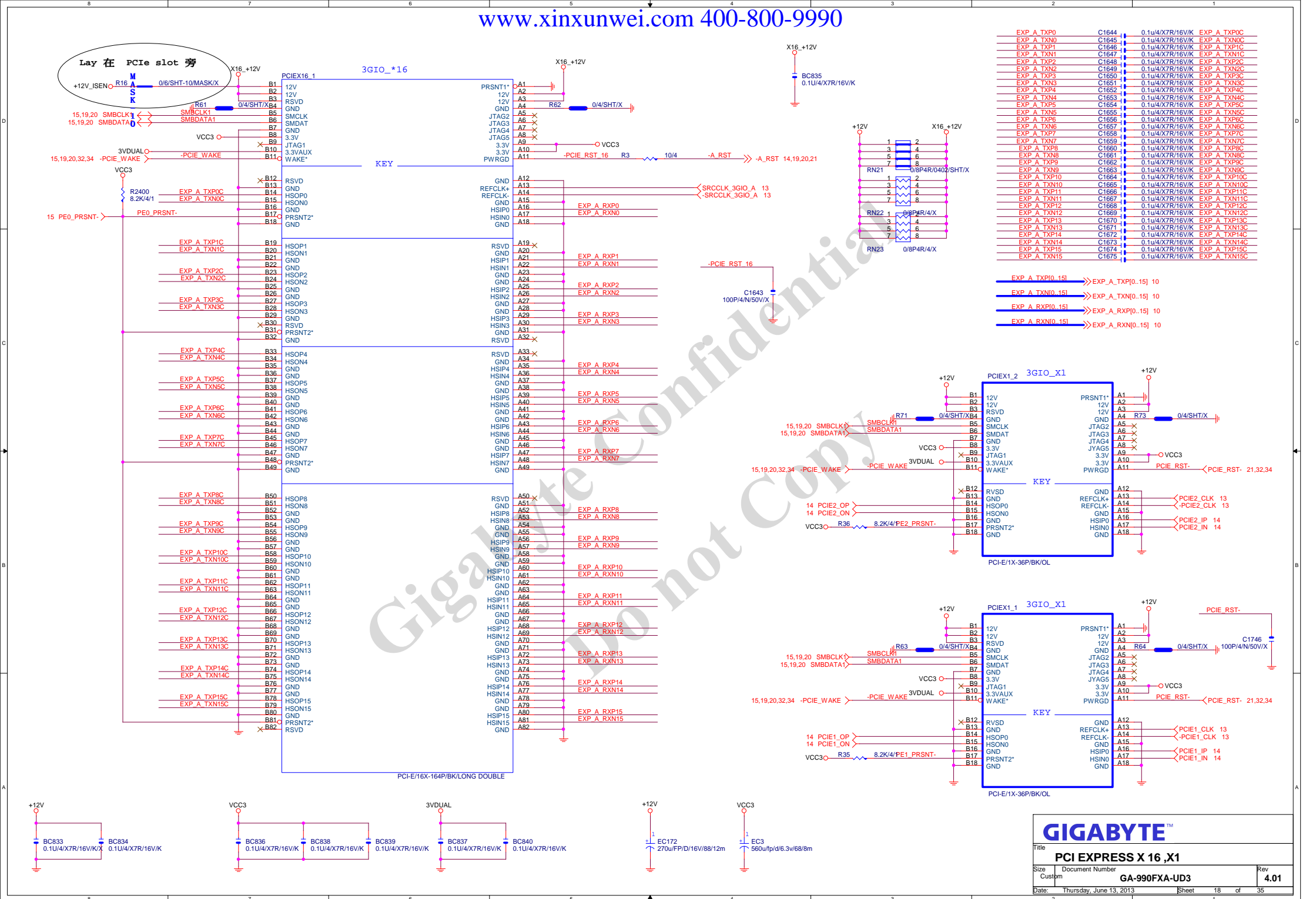
PLACE SATA AC COUPLING
CAPS CLOSE TO SB850

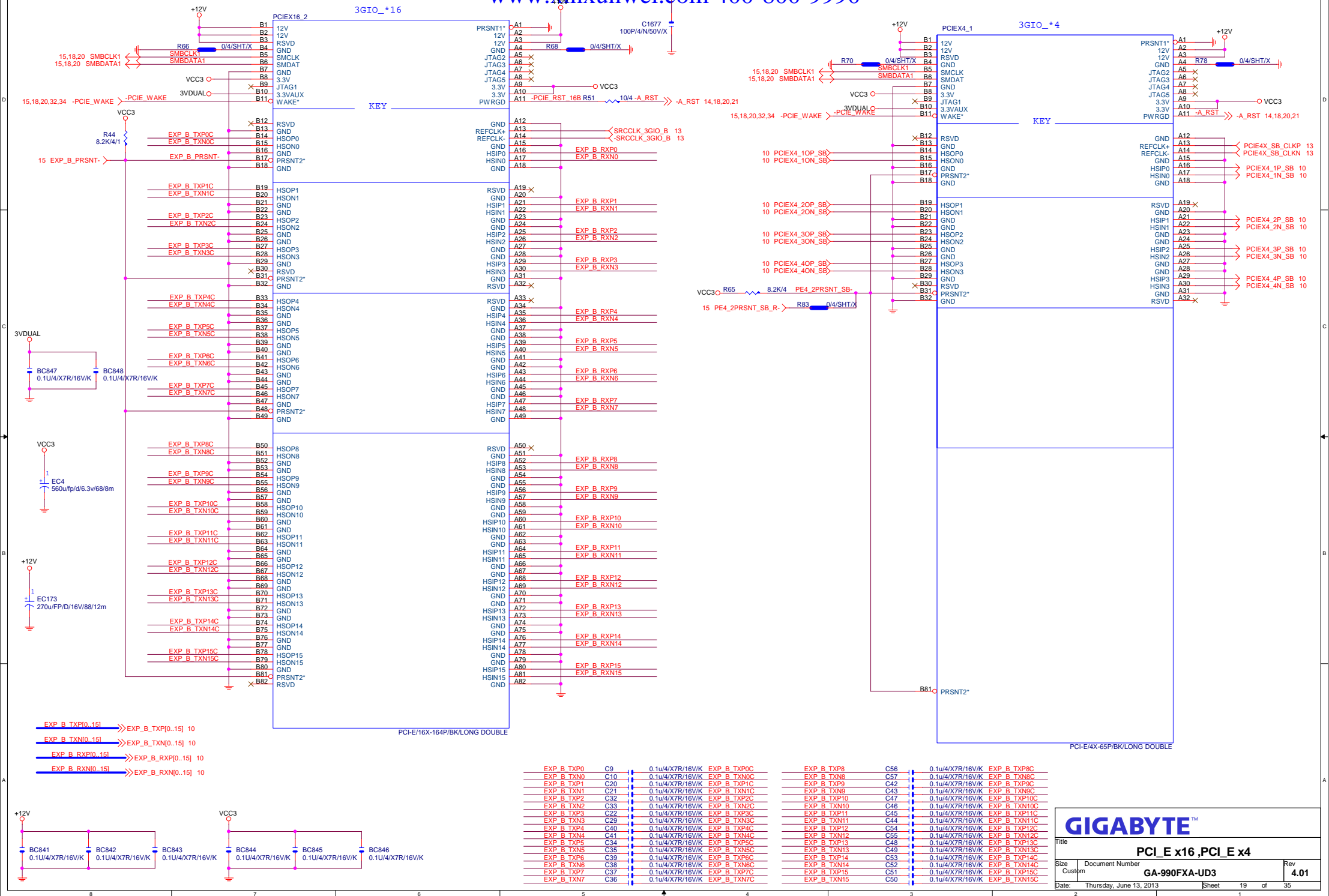


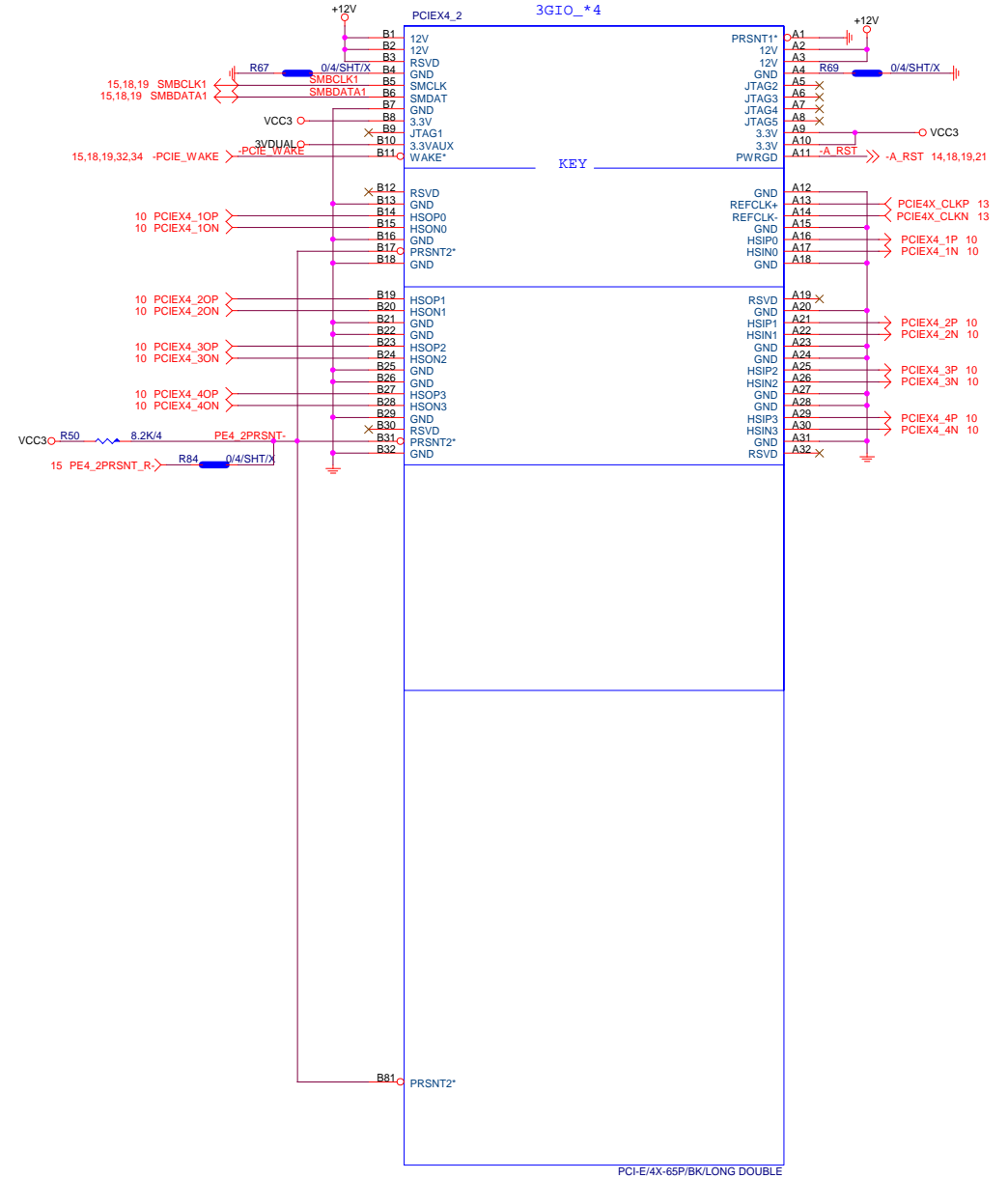
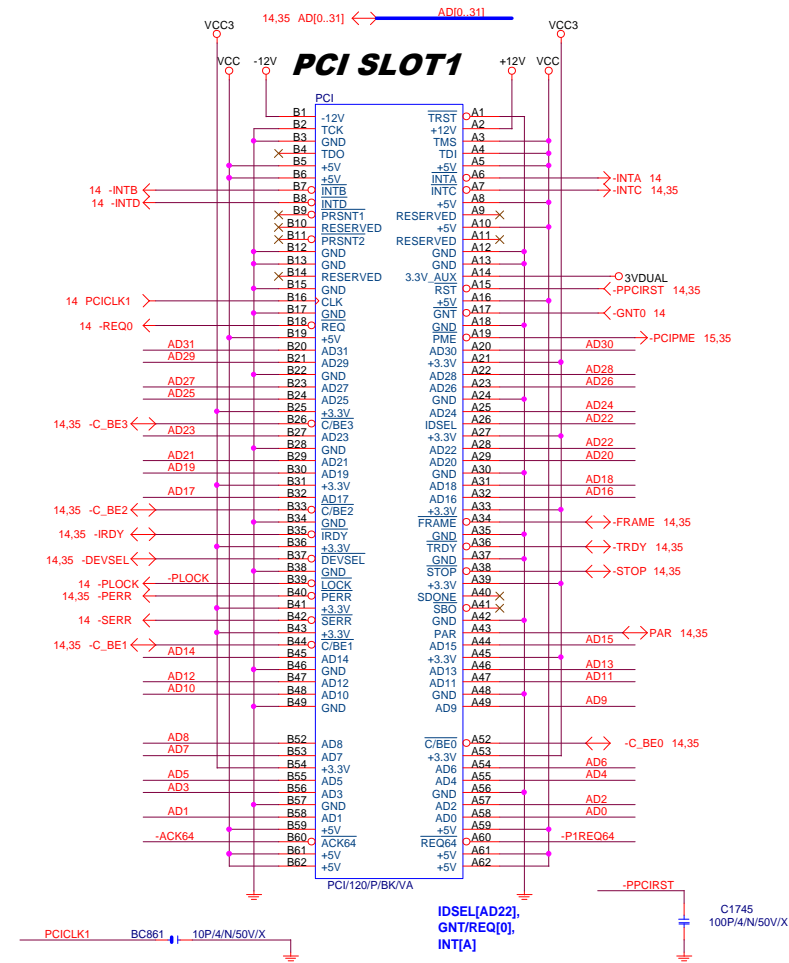
GIGABYTE

Title	ATI SB950 SATA/IDE/HWM/SPI		
Size	Document Number	Rev	4.01
Custom	GA-990FXA-UD3		
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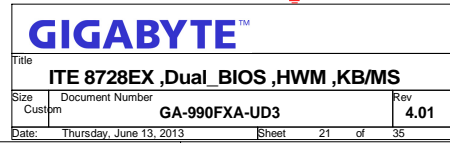




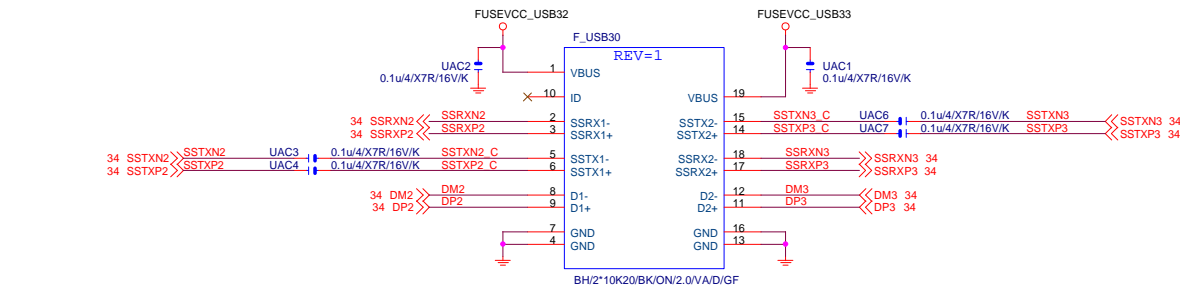
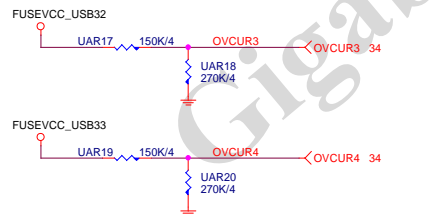
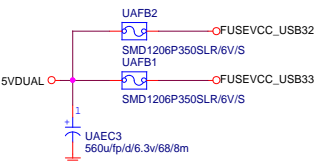
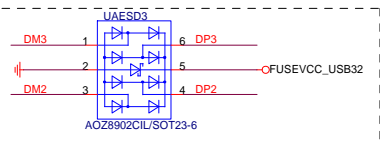
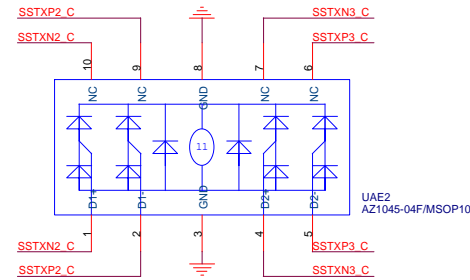
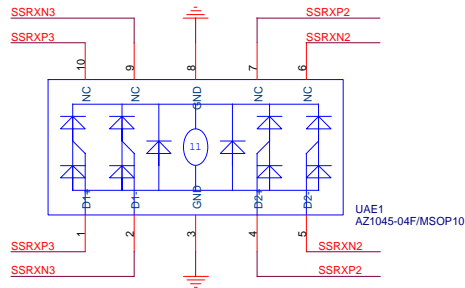
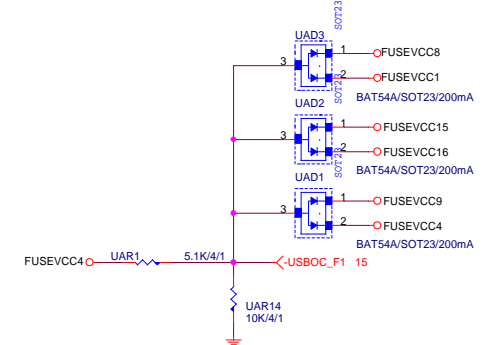
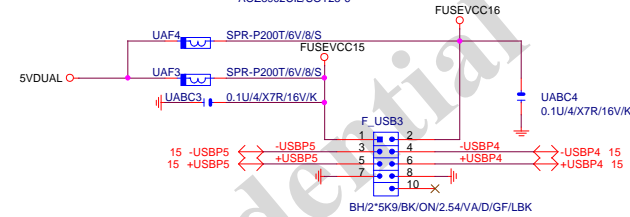
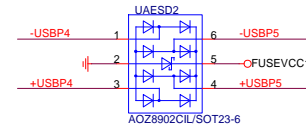
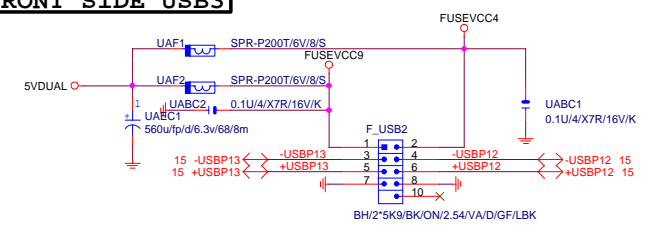
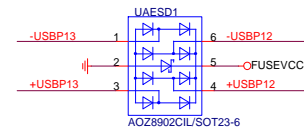
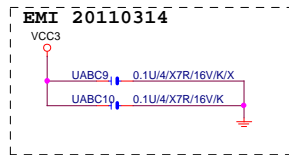


PCI SLOT1**GIGABYTE™**

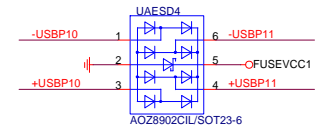
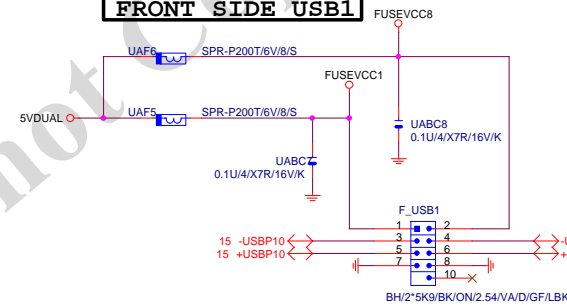
Title		
PCI SLOT,PCIEx4		
Size	Document Number	Rev
Custm	GA-990FXA-UD3	4.01
Date:	Thursday, June 13, 2013	Sheet 20 of 35



FRONT SIDE USB3



FRONT SIDE USB1



GIGABYTE

COM/LPT/F_USB

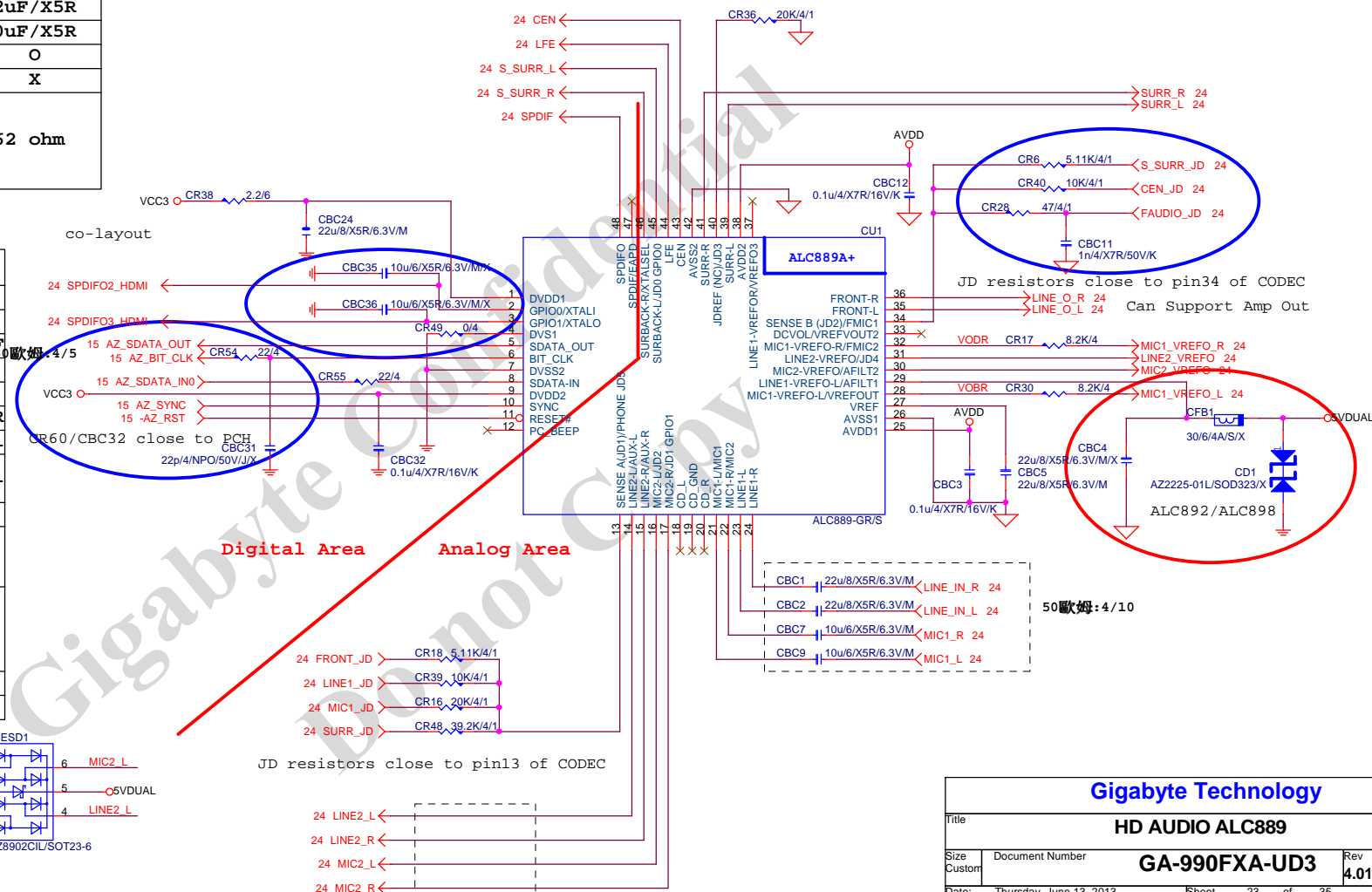
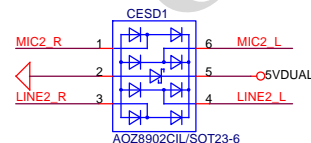
Size: Custom
Document Number: GA-990FXA-UD3
Date: Thursday, June 13, 2013
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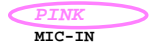
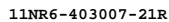
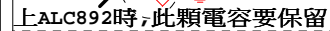
Rev: 4.01

	ALC889	ALC889B	ALC898/ALC892
CR65	O	O	X
CBC35	X	X	10uF/X5R
CBC39	X	10uF/X5R	X
CR31	O	X	O
CR66	X	O	X
CBC1/CBC2	22uF/X5R	22uF/X5R	22uF/X5R
CBC5/CBC6/CBC9/CBC11	10uF/X5R	10uF/X5R	10uF/X5R
CR51/CD1/CBC7	X	X	O
CD2/CD3/CQ3/CQ5	O	O	X
CR5/CR8/CR1/CR14/ CR17/CR22/CR45/CR33/ CR47/CR40/CR26/CR37/ CR13/CR11/CR57/CR53	62 ohm	62 ohm	62 ohm

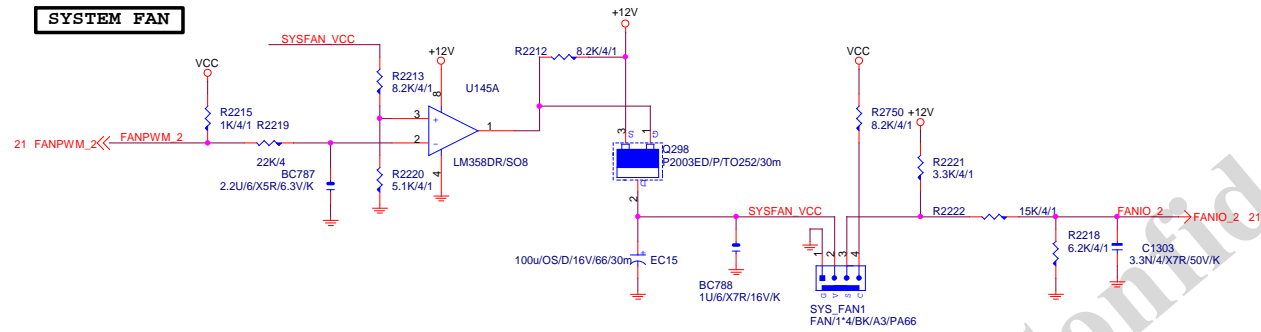
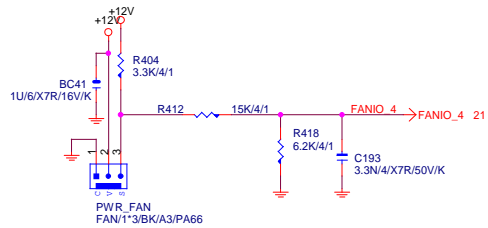
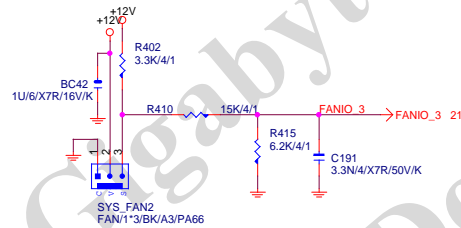
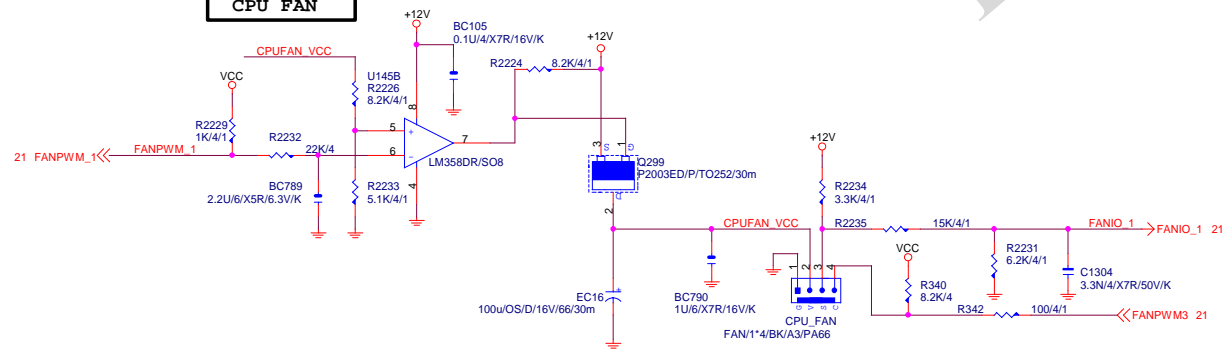
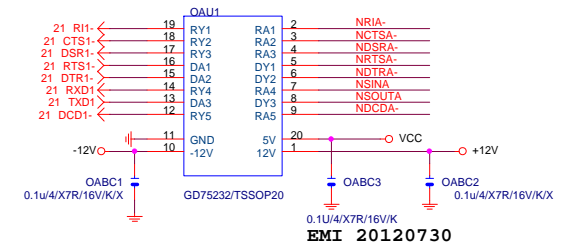
ALC889/VT2021 Colay

	ALC889	VT2021
CR49	O	O
CBC36	X	X
CR28/CBC11	47ohm+1nF	47ohm+1nF
CR52	O	O
CBC1/CBC2	22uF/X5R	10uF/X5R
CR36	20K/4/1	5.1K/4/1
CR17/CR30/ CR25/CR15/CR12/CR3	8.2K/4	3.3K/4/1
CBC38/CBC39	X	X
CR10/CR8/CR20/CR45/ CR42/CR51/CR43/CR22/ CR27/CR26	22K/4	10K/4/1
CR7/CR9/CR5/CR13/ CR29/CR32/CR46/CR19/ CR50/CR41/CR21/CR47 CR2/CR11/CR14/CR24	62 ohm	75 ohm
CFB1/CD1/CBC4	X	X
CD2/CD3/CQ3/CQ4	O	O

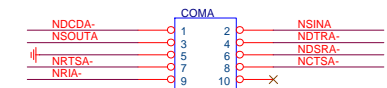
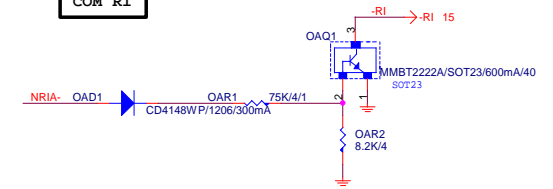




Title			
AUDIO JACK			
Size Custom	Document Number	GA-990FXA-UD3	Rev 4.01
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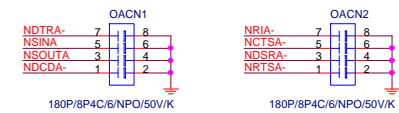
SYSTEM FAN**POWER FAN****SYSTEM FAN2****CPU FAN****COMA**

EMI 20120730

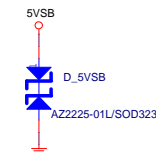
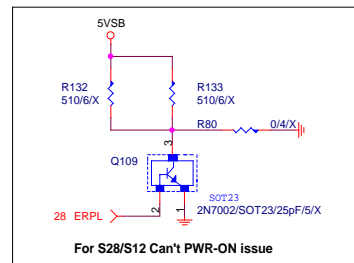
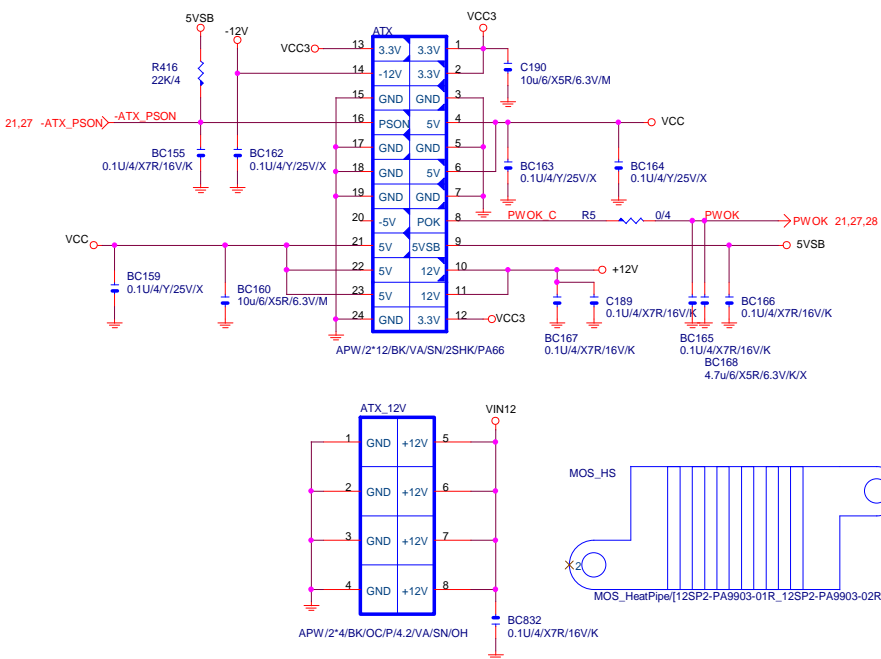
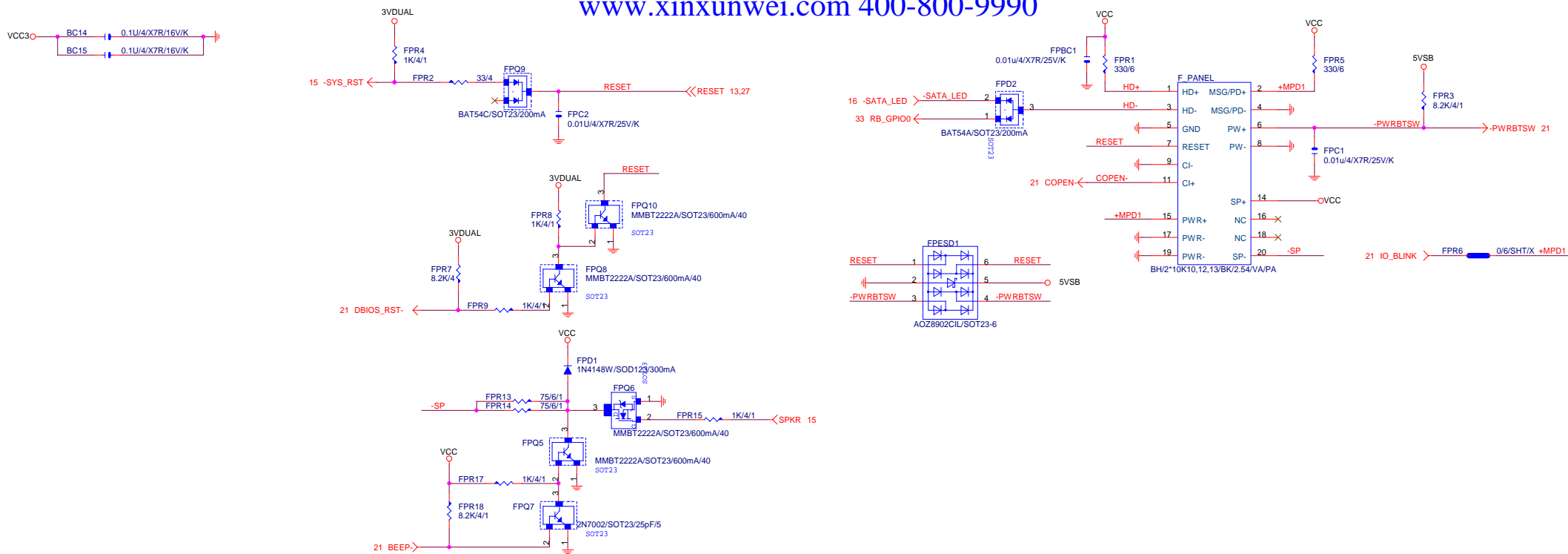
COM RI

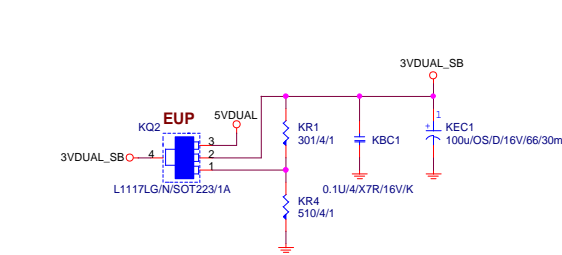
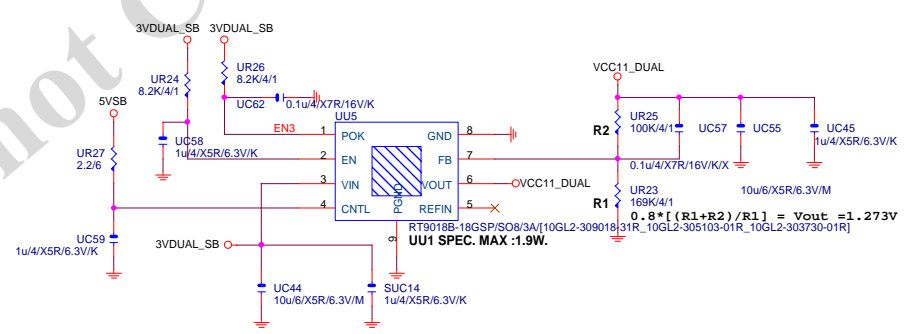
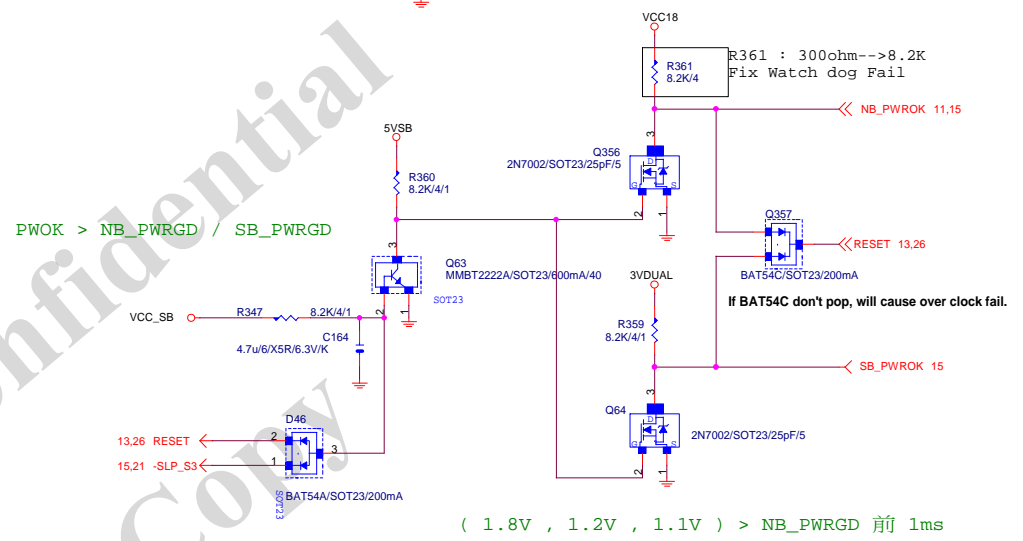
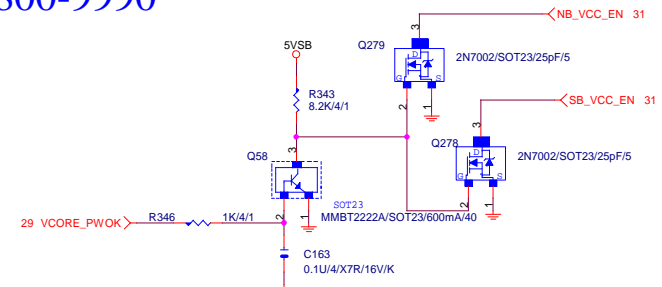
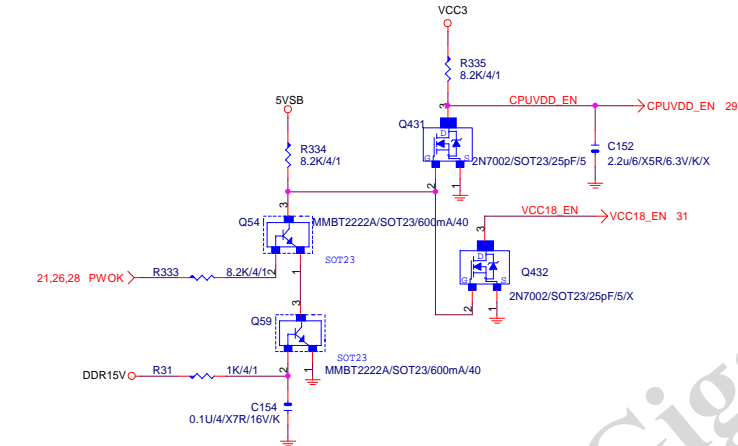
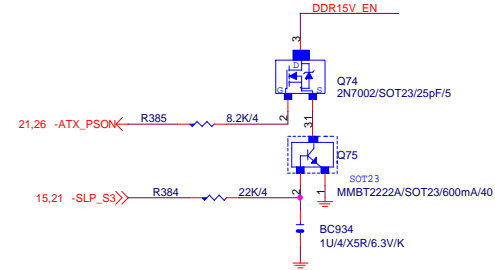
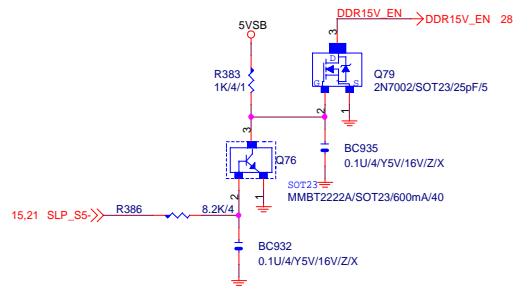
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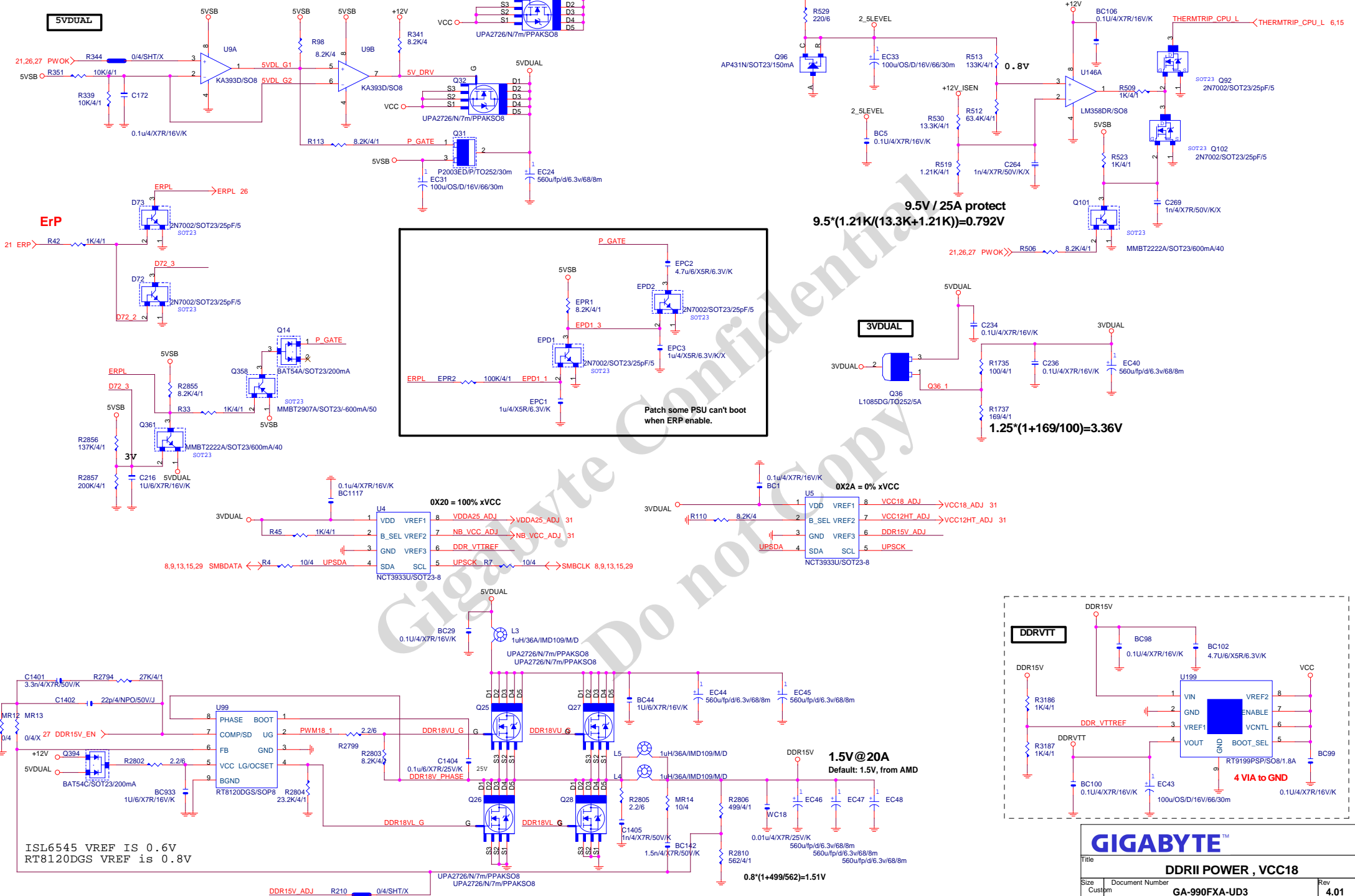
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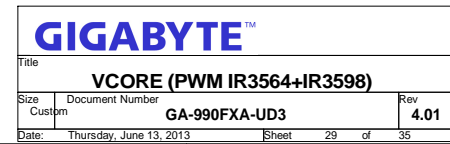
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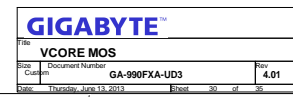


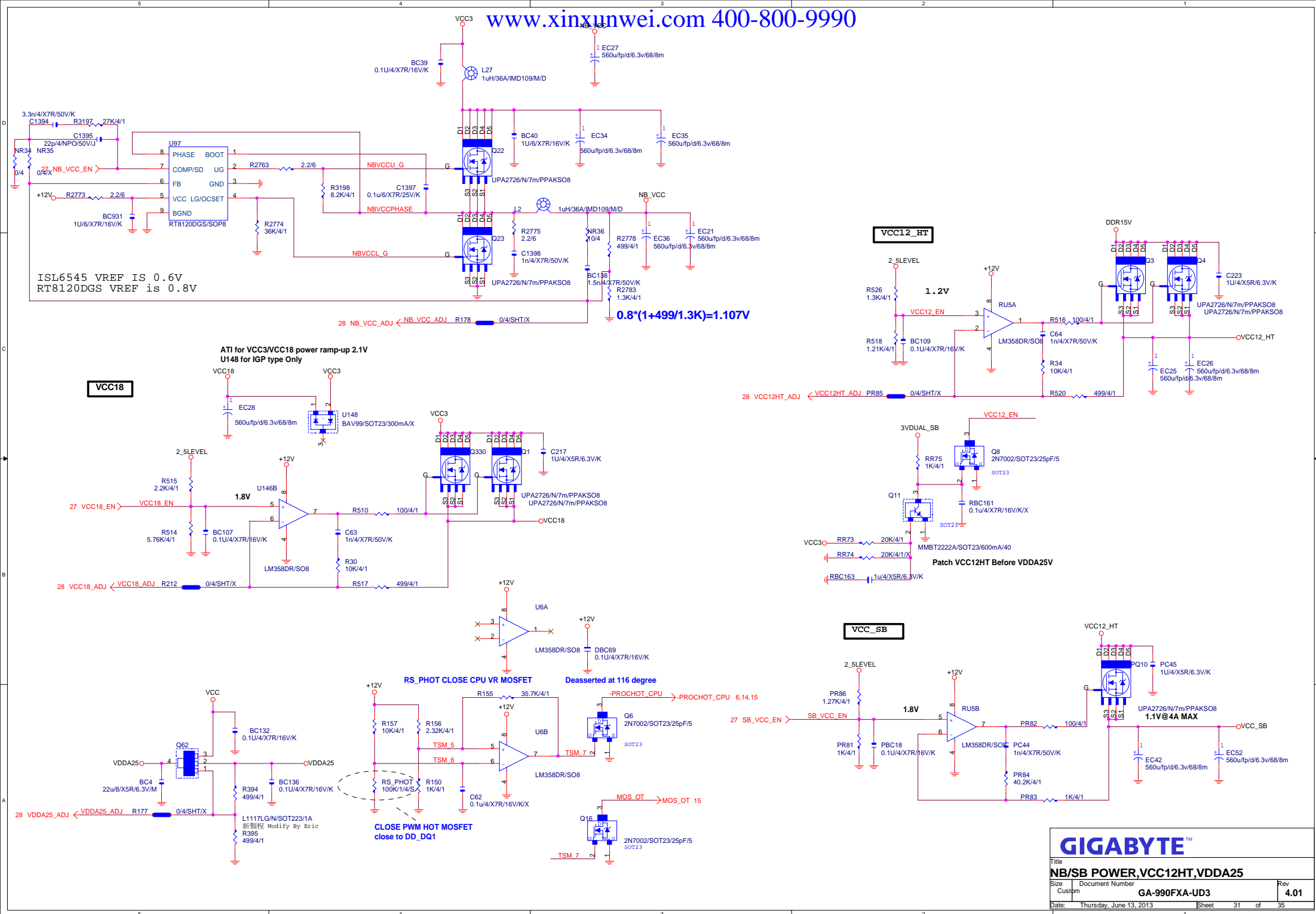


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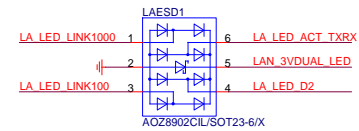
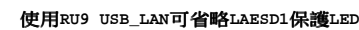
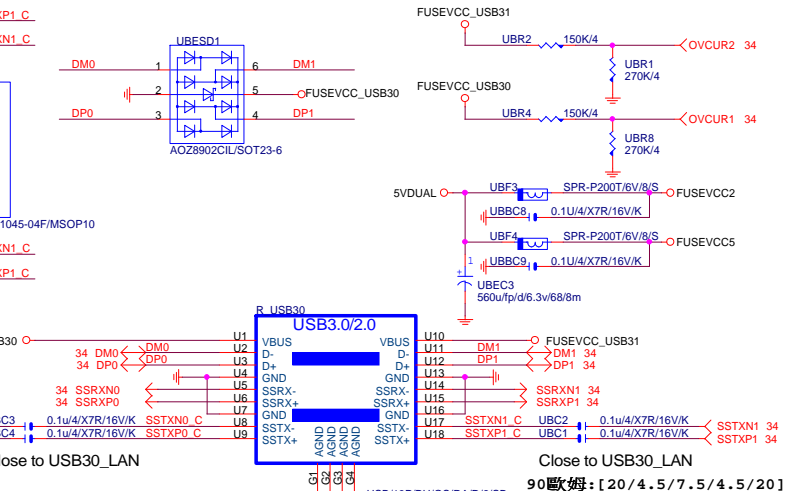
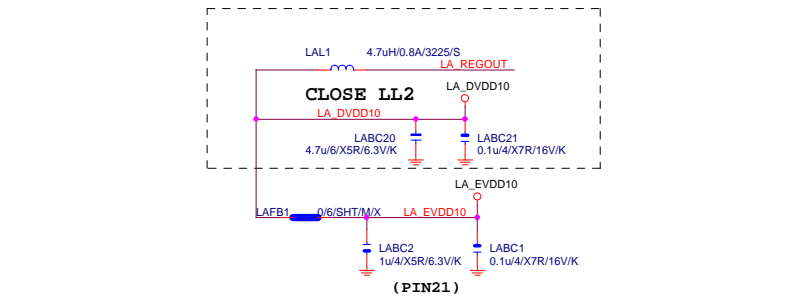
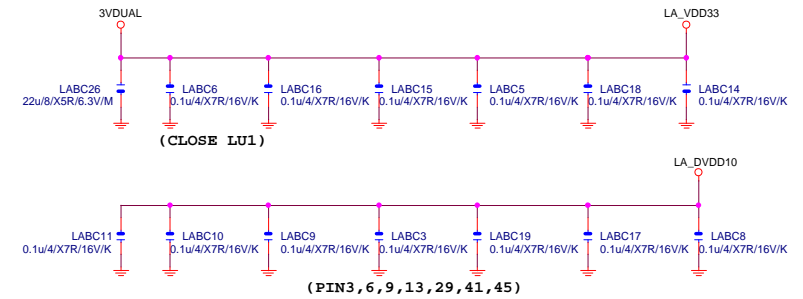
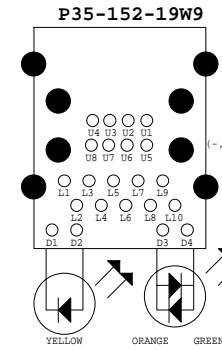
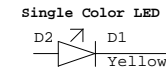
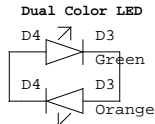
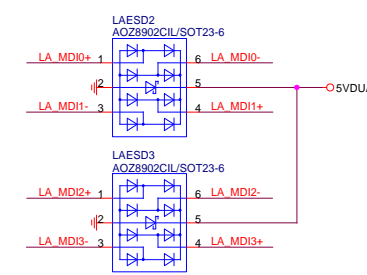
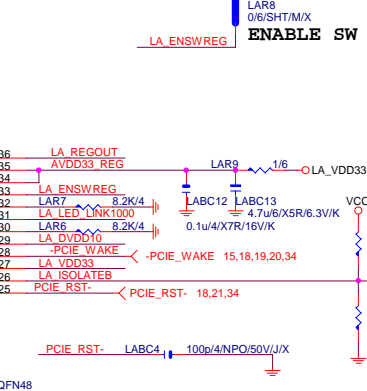
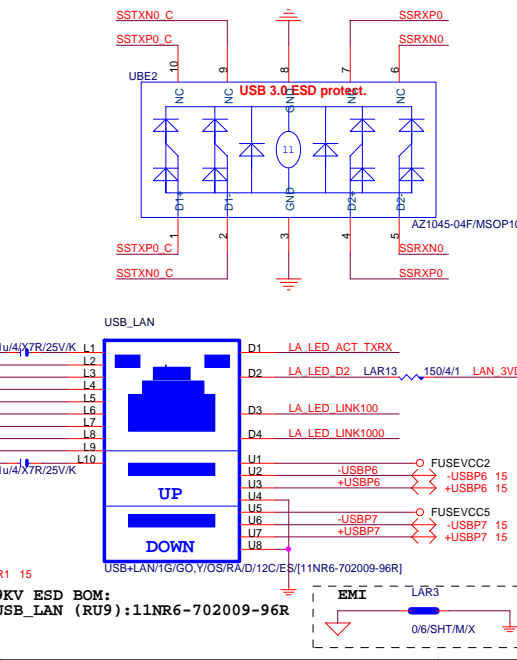
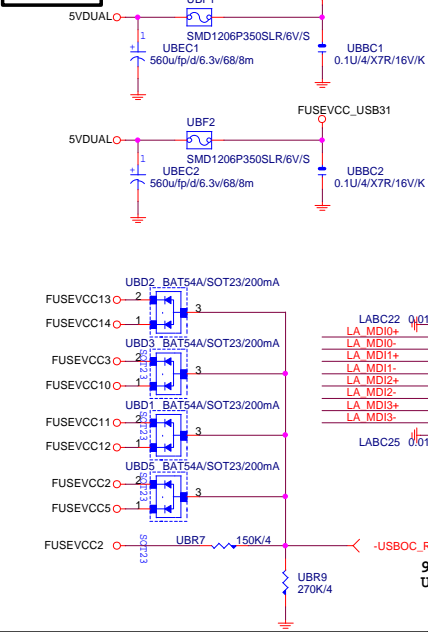






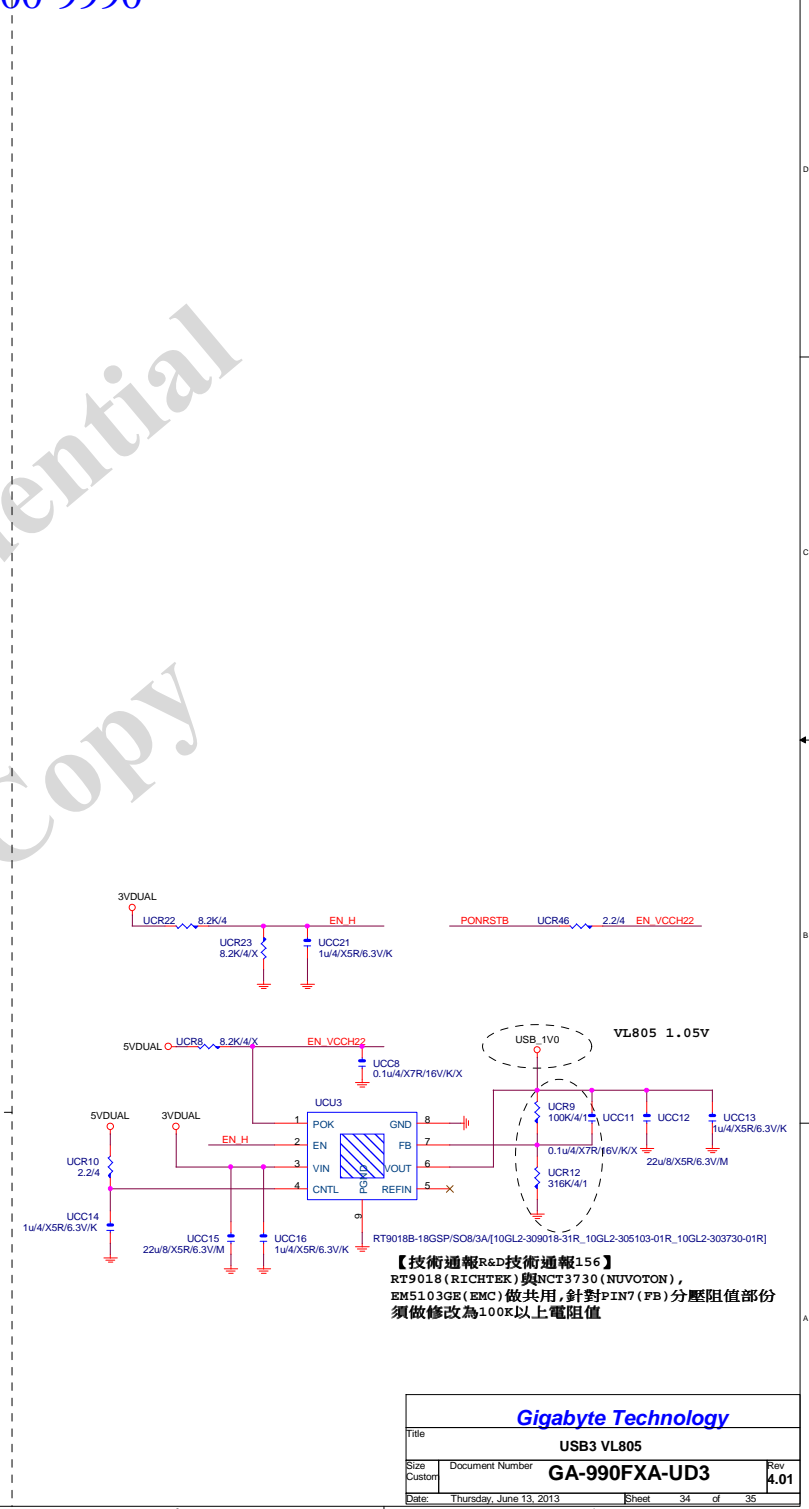


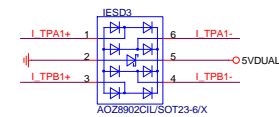
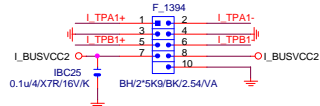
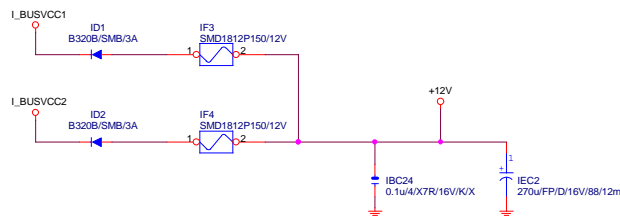
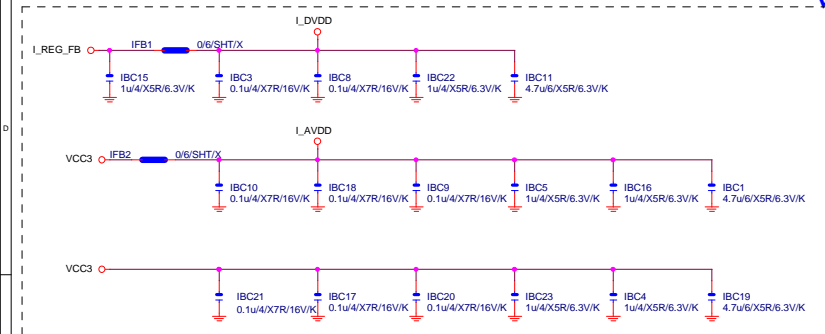
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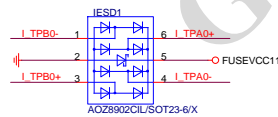
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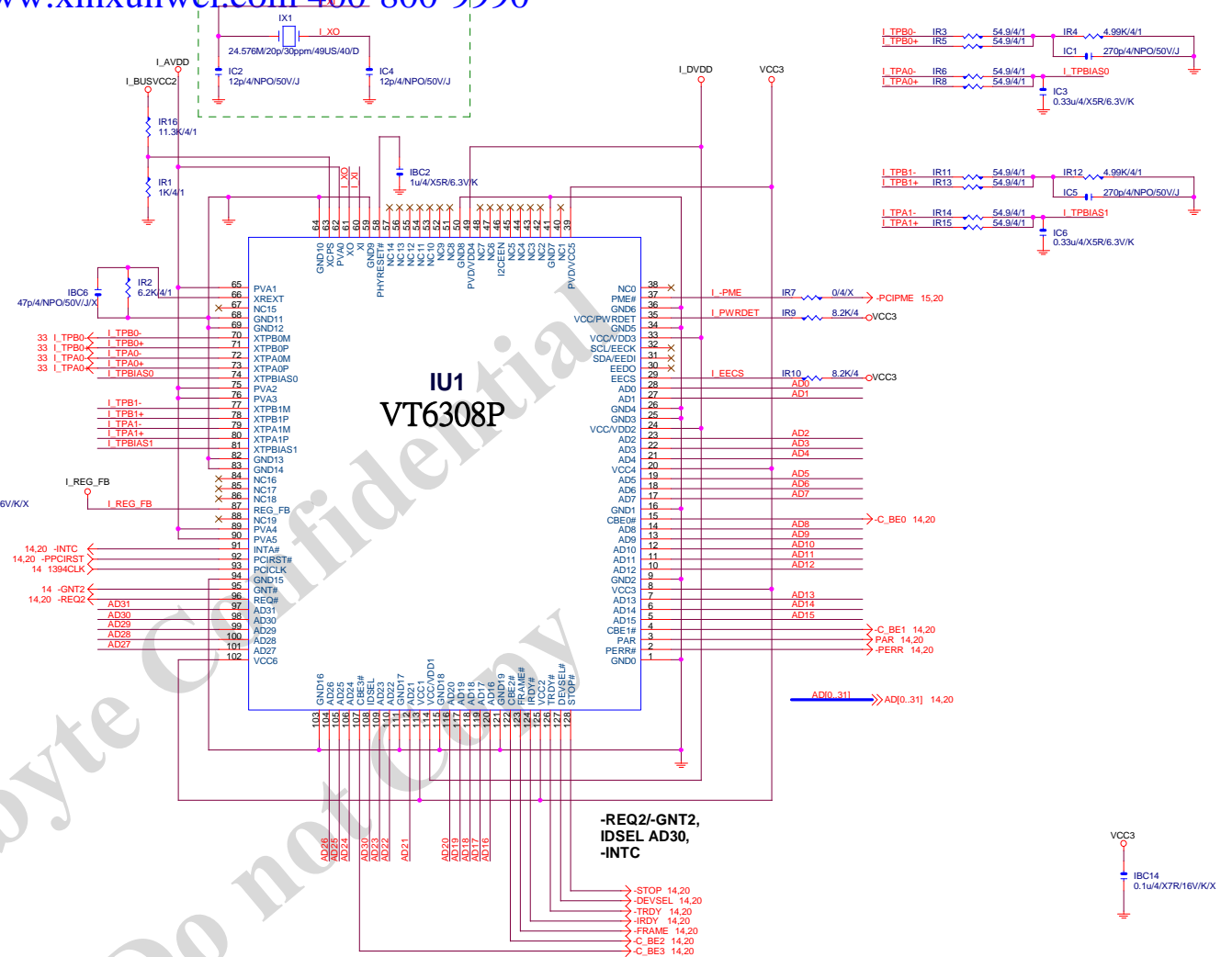




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Place close to Header or connector



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IDSEL AD30,
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